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74

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Format for Search Results:
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Where have you searched? EAST / NPL

ATTACH YOUR EAST/WEST SEARCH STRATEGY

A Fast and Focused SEARCH is a 1-2 hour NPL search on a very targeted art area using specific concepts, Keywords, synonyms, or acronyms.

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Please attach a copy of the pertinent information.

receivers - "symmetric offsets"

STIC Searcher Virgil Tyler Phone X8534

Date picked up 3/22/07 Date completed 3/22/07

STIC FAST + FOLLOW)

SEARCH

[File 2] **INSPEC** 1898-2007/Mar W2
(c) 2007 Institution of Electrical Engineers. All rights reserved.

[File 6] **NTIS** 1964-2007/Mar W3
(c) 2007 NTIS, Intl Cpyrght All Rights Res. All rights reserved.

[File 8] **Ei Compendex(R)** 1884-2007/Mar W2
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[File 34] **SciSearch(R) Cited Ref Sci** 1990-2007/Mar W3
(c) 2007 The Thomson Corp. All rights reserved.

[File 35] **Dissertation Abs Online** 1861-2007/Feb
(c) 2007 ProQuest Info&Learning. All rights reserved.

[File 56] **Computer and Information Systems Abstracts** 1966-2007/Mar
(c) 2007 CSA. All rights reserved.

[File 57] **Electronics & Communications Abstracts** 1966-2007/Mar
(c) 2007 CSA. All rights reserved.

[File 65] **Inside Conferences** 1993-2007/Mar 22
(c) 2007 BLDSC all rts. reserv. All rights reserved.

[File 94] **JICST-EPlus** 1985-2007/Mar W4
(c)2007 Japan Science and Tech Corp(JST). All rights reserved.
**File 94: JICST will be removed from all vendors on March 31, 2007. Please contact the Knowledge Center for alternative files.*

[File 95] **TEME-Technology & Management** 1989-2007/Mar W3
(c) 2007 FIZ TECHNIK. All rights reserved.

[File 99] **Wilson Appl. Sci & Tech Abs** 1983-2007/Feb
(c) 2007 The HW Wilson Co. All rights reserved.

[File 144] **Pascal** 1973-2007/Mar W2
(c) 2007 INIST/CNRS. All rights reserved.

[File 256] **TecInfoSource** 82-2007/Oct
(c) 2007 Info.Sources Inc. All rights reserved.

[File 434] **SciSearch(R) Cited Ref Sci** 1974-1989/Dec
(c) 2006 The Thomson Corp. All rights reserved.

[File 583] **Gale Group Globalbase(TM)** 1986-2002/Dec 13
(c) 2002 The Gale Group. All rights reserved.
**File 583: This file is no longer updating as of 12-13-2002.*

[File 603] **Newspaper Abstracts** 1984-1988
(c)2001 ProQuest Info&Learning. All rights reserved.
**File 603: This is a closed file.*

[File 483] **Newspaper Abs Daily** 1986-2007/Mar 23
(c) 2007 ProQuest Info&Learning. All rights reserved.

[File 248] **PIRA** 1975-2007/Feb W4
(c) 2007 Pira International. All rights reserved.

```
Set     Items   Description
S1      29771   S COMPARATOR?? OR COMPARATOR??()CIRCUIT???
S2          0   S (PAM()4 OR (FET OR FIELD()EFFECT()TRANSISTOR??)(3N)CMOS)(3N)S1
S3       2648   S (PLURAL? OR MULTI OR MULTIPLE OR MANY SEVERAL OR MORE(1N)ONE OR TWO
OR 2 OR SECOND OR NUMEROUS OR THIRD OR THREE OR 3 OR PAIR??)(3N)(S1 OR S2)
S4          0   S LOAD(3N)(RESISTANCE OR RESISTOR?? OR IMPEDANCE)(3N)S3
S5          0   S (CENTER()TAP? OR NODE?? OR SLICE??)(3N)S4
```

```
S6          0   S (INTERCONNECT?? OR COUPL? OR WIRE?? OR CONNECT??? OR ATTACH???? OR
LINK??? OR JOIN??? OR INTEGA??? OR OPERATIVE?)(3N)(S4 OR S5)
S7      81159   S VOLT???(3N)(OFFSET???? OR OFF()SET???? OR THRESHOLD OR FACTORS OR
VALUE OR MAX OR MAXIMUM OR NUMBER)
S8      14964   S AU=(BROWN, W? OR BROWN W?)
S9         10   S S3(3N)S7
S10         8   RD  (unique items)
S11         5   S S10 NOT PY>2003
S12         4   S S3 AND S8
S13         4   S S12 NOT S10
S14         2   RD  (unique items)
S15         1   S S14 NOT PY>2002
S16         0   S S15 NOT PLACEBO
S17        40   S S7 AND S8
S18         0   S S17(20N)S1
S19         0   S S17(40N)S1
```

11/3,K/1 (Item 1 from file: 2) **Links**
INSPEC

08993328 **INSPEC Abstract Number:** B2004-07-1150D-001
Title: Low power CMOS dynamic latch comparators
Author Uthaichana, P.; Leelarasmee, E.
Author Affiliation: Electr. Eng. Dept., Chulalongkorn Univ., Bangkok, Thailand
Conference Title: IEEE TENCON 2003. Conference on Convergent Technologies for the Asia-Pacific Region (IEEE Cat. No.03CH37503) **Part** Vol.2 p. 605-8 Vol.2
Publisher: Allied Publishers Pvt. Ltd , New Delhi, India
Publication Date: 2003 **Country of Publication:** India xxxviii+1626 pp.
ISBN: 0 7803 8162 9 **Material Identity Number:** XX-2004-00155
Conference Title: IEEE TENCON 2003. Conference on Convergent Technologies for the Asia-Pacific Region
Conference Sponsor: IEEE Region 10
Conference Date: 15-17 Oct. 2003 **Conference Location:** Bangalore, India
Language: English
Subfile: B

Abstract: ...charge sharing technique yields lowest power consumption of 90 mu W at 100 MHz. All **three comparators** have an **offset voltage** in the range of 30-150 mV.

11/3,K/2 (Item 2 from file: 2) **Links**
Fulltext available through: USPTO Full Text Retrieval Options
INSPEC

08925521 **INSPEC Abstract Number:** B2004-05-1265-003
Title: Self floats study for threshold voltage of 555 timer
Author Liu Zhi-Yi; Cao Shu-Fu
Author Affiliation: Coll. of Inf. Sci. & Eng., Hebei Univ. of Sci. & Technol., China
Journal: Hebei Journal of Industrial Science & Technology vol.20, no.6 p. 42-4
Publisher: Editorial Committee of Hebei J. Ind. Sci. & Technol ,
Publication Date: Nov. 2003 **Country of Publication:** China
CODEN: HGKEFI **ISSN:** 1008-1534
SICI: 1008-1534(200311)20:6L.42:SFST;1-W
Material Identity Number: H477-2003-006
Language: Chinese
Subfile: B

Abstract: ...out feeding back to input for voltage apron string, forms deferent DS feedback, and holds **threshold voltage** inside **two comparators** to float along with. Using the theory of feedback and threshold voltage self float, and...

11/3,K/3 (Item 3 from file: 2) **Links**
Fulltext available through: USPTO Full Text Retrieval Options

INSPEC

03322593 **INSPEC Abstract Number:** B84051499
Title: Analysis and evaluation of CMOS chopper type comparator
Author Kuboki, S.; Hirayama, T.; Kato, K.
Author Affiliation: Hitachi Res. Lab., Hitachi Ltd., Hitachi, Japan
Journal: Transactions of the Institute of Electronics and Communication Engineers of Japan, Part C vol.J67C, no.5 p. 443-50

Publication Date: May 1984 **Country of Publication:** Japan
CODEN: DTGCAY **ISSN:** 0373-6113
Language: Japanese
Subfile: B
Abstract: ...are introduced. The relationship of comparison speed to circuit parameter is then clarified. Using a **3** mu m CMOS **comparator**, **offset voltage** of 0.5 mV and sampling time of 190 ns are obtained. Finally, design philosophy...

11/3,K/4 (Item 4 from file: 2) **Links**
Fulltext available through: USPTO Full Text Retrieval Options
INSPEC

02052113 **INSPEC Abstract Number:** B77020481, C77012821
Title: A method for improving the linearity of reset-type voltage-to-frequency converters
Author Taniguchi, K.; Sakai, T.
Author Affiliation: Faculty of Engng., Fukui Univ., Fukui, Japan
Journal: System - Computers - Controls vol.6, no.5 p. 1-7

Publication Date: Sept.-Oct. 1975 **Country of Publication:** USA
CODEN: SYCCBB **ISSN:** 0096-8765
Language: English
Subfile: B C
Abstract: ...1) by increasing the minimum value of the sweep voltage with the input voltage, or (**2**) by controlling the **comparator threshold voltage** with the input voltage. Good linearity can be realized up to high frequencies if the...

11/3,K/5 (Item 5 from file: 2) **Links**
INSPEC

01078479 **INSPEC Abstract Number:** B70000388
Title: High and low voltage level threshold circuit employing two differential amplifier comparators
Inventor Berry, A.D.
Assignee GEC Ltd
Patent Number: US 3428827 **Issue Date:** 690218
Application Date: 650701
Priority Application Number: GB 27552/64 **Priority Application Date:** 640703
Country of Publication: USA
Language: English
Subfile: B
Title: High and low voltage level threshold circuit employing two differential amplifier comparators

[File 344] **Chinese Patents Abs** Jan 1985-2006/Jan

[File 347] **JAPIO** Dec 1976-2006/Nov(Updated 070228)

[File 350] **Derwent WPIX** 1963-2006/UD=200719

**File 350: DWPI has been enhanced to extend content and functionality of the database. For more info, visit http://www.dialog.com/dwpi/.*

[File 371] **French Patents** 1961-2002/BOPI 200209

**File 371: This file is not currently updating. The last update is 200209.*

```
Set     Items   Description
S1     212003   S COMPARATOR?? OR COMPARATOR??()CIRCUIT???
S2          4   S (PAM()4 OR (FET OR FIELD()EFFECT()TRANSISTOR??)(3N)CMOS)(3N)S1
S3      42406   S (PLURAL? OR MULTI OR MULTIPLE OR MANY SEVERAL OR MORE(1N)ONE OR TWO
OR 2 OR SECOND OR NUMEROUS OR THIRD OR THREE OR 3 OR PAIR??)(3N)(S1 OR S2)
S4         28   S LOAD(3N)(RESISTANCE OR RESISTOR?? OR IMPEDANCE)(3N)S3
S5          2   S (CENTER()TAP? OR NODE?? OR SLICE??)(3N)S4
S6          2   S (INTERCONNECT?? OR COUPL? OR WIRE?? OR CONNECT??? OR ATTACH???? OR
LINK??? OR JOIN??? OR INTEGA??? OR OPERATIVE?)(3N)(S4 OR S5)
S7     113161   S VOLT???(3N)(OFFSET???? OR OFF()SET???? OR THRESHOLD OR FACTORS OR
VALUE OR MAX OR MAXIMUM OR NUMBER)
S8        879   S AU=(BROWN, W? OR BROWN W?)
S9          2   S S5 NOT S2
S10         2   S S6 NOT (S2 OR S5)
S11         1   S S4(3N)S7
S12         1   S S11 NOT (S2 OR S5 OR S10)
S13         2   S S4(S)S7
S14         1   S S13 NOT (S2 OR S5 OR S10 OR S12)
S15        22   S S4 NOT (S2 OR S5 OR S10 OR S12 OR S14)
S16        21   S S15 NOT AD=20030708:20070322/PR
S17         5   S S16 AND (IC=H04L? OR IC=H03K?)
S18         0   S S16 AND SYMMETRIC()OFFSET?
S19        16   S S16 NOT (S2 OR S5 OR S10 OR S12 OR S14 OR S17)
S20        97   S S3(3N)(CENTER()TAP? OR SLICE?? OR CHOP?)
S21         5   S S20(3N)(INTERCONNECT?? OR COUPL? OR WIRE?? OR CONNECT??? OR
ATTACH???? OR LINK??? OR JOIN??? OR INTEGA??? OR OPERATIVE?)
S22         5   S S21 NOT (S2 OR S5 OR S10 OR S12 OR S14 OR S17 OR S19)
S23         1   S S20 AND S8
S24         1   S S20(3N)S7
S25         0   S S24 NOT S20
S26         0   S (LOAD(3N)(RESISTANCE OR RESISTOR?? OR IMPEDANCE))(3N)S20
S27         1   S (LOAD(3N)(RESISTANCE OR RESISTOR?? OR IMPEDANCE))(S)S20
S28         1   S S27 NOT S24
S29         0   S S28 NOT (S2 OR S5 OR S10 OR S12 OR S14 OR S17 OR S19)
```

2/3,K/1 (Item 1 from file: 350) **Links**
Derwent WPIX

0005546818
WPI Acc no: 1991-151446/199121
XRPX Acc No: N1991-116142
CMOS FET inverter chopper type comparator - has current cut-off switch connected in series to CMOS FETs and turned off during standby session NoAbstract Dwg 1/5

Patent Assignee: OKI ELECTRIC IND CO LTD (OKID)
Inventor: OYA M

Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
JP 3085013	A	19910410	JP 1989221064	A	19890828	199121	B

Priority Applications (no., kind, date): JP 1989221064 A 19890828

CMOS FET inverter chopper type comparator -

2/3,K/2 (Item 2 from file: 350) **Links**
Derwent WPIX

0005373402
WPI Acc no: 1990-373373/199050
XRPX Acc No: N1990-284693
CMOS FET signal level comparator circuit for microcomputer - has circuit for comparing common-mode input voltage with reference voltage NoAbstract Dwg 1/4
Patent Assignee: NEC CORP (NIDE)
Inventor: IKUTA J

Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
JP 2271712	A	19901106	JP 198994006	A	19890412	199050	B

Priority Applications (no., kind, date): JP 198994006 A 19890412

CMOS FET signal level comparator circuit for microcomputer...

2/3,K/3 (Item 3 from file: 350) **Links**
Derwent WPIX

0004871544 *Drawing available*
WPI Acc no: 1989-251326/198935
CMOS FET chopper type comparator - has clock connected to parallel-connected P channel FET's via double inverters NoAbstract Dwg 3/6
Patent Assignee: RICOH KK (RICO)
Inventor: MURAKAMI H

Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
JP 1181221	A	19890719	JP 19886568	A	19880113	198935	B

Priority Applications (no., kind, date): JP 19886568 A 19880113

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
JP 1181221	A	JA	4		

CMOS FET chopper type comparator -

2/3,K/4 (Item 4 from file: 350) **Links**
Derwent WPIX

0002885610
WPI Acc no: 1983-F2214K/198316
CMOS FET voltage comparator circuit - uses differential amplifier with control transistor connected between commonly connected sources of latch transistors and reference voltage terminal
Patent Assignee: NIPPON ELECTRIC CO (NIDE)
Inventor: YUGAWA A; YUKAWA A

Patent Family (2 patents, 2 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
JP 58040918	A	19830310	JP 1981138946	A	19810903	198316	B
US 4511810	A	19850416	US 1982414724	A	19820903	198518	E

Priority Applications (no., kind, date): JP 1981138946 A 19810903

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
JP 58040918	A	JA	9	8	

CMOS FET voltage comparator circuit -

9/3,K/1 (Item 1 from file: 350) **Links**
Derwent WPIX

0014772816 *Drawing available*
WPI Acc no: 2005-120481/200513
XRPX Acc No: N2005-103925
Data slicer for use in data transmission system, has three comparator circuits, each establishing respective threshold, where two of comparator circuits have symmetrical offsets and include load resistor that has center tap
Patent Assignee: BROWN W W (BROW-I)
Inventor: BROWN W W

Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 20050008099	A1	20050113	US 2003616214	A	20030708	200513	B

Priority Applications (no., kind, date): US 2003616214 A 20030708

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
US 20050008099	A1	EN	5	1	

...
for use in data transmission system, has three comparator circuits, each establishing respective threshold, where two of comparator circuits have symmetrical offsets and include load resistor that has center tap

9/3,K/2 (Item 2 from file: 350) **Links**
Derwent WPIX

0007129336 *Drawing available*
WPI Acc no: 1995-161446/199521
XRPX Acc No: N1995-126685
Receiver squelch circuit with adjustable threshold - has input device responsive to incoming system for generating decision signal when DC voltage level crosses set threshold voltage level
Patent Assignee: NAT SEMICONDUCTOR CORP (NASC)
Inventor: TRAN T V

Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 5408694	A	19950418	US 1992826786	A	19920128	199521	B
			US 1993112653	A	19930826		

Priority Applications (no., kind, date): US 1992826786 A 19920128; US 1993112653 A 19930826

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
US 5408694	A	EN	7	3	Continuation of application	US 1992826786

Original Publication Data by Authority

...
Claims:
second load resistor and its non-inverting input connected to the output-side node of **the** first load resistor; **and (k)** second comparator **means having** its inverting input connected to the input-side of the first load resistor and its...

10/3,K/1 (Item 1 from file: 350) **Links**
Derwent WPIX

0010121865
WPI Acc no: 2000-429676/200037
XRPX Acc No: N2000-320480
Amplifier using adaptive pulse-width modulation
Patent Assignee: UNIV NOVCH TECH (NCPO)
Inventor: LACHIN V I; MALINA A K; SOLOMENTSEV K YU

Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
RU 2138117	C1	19990920	RU 1998122575	A	19981215	200037	B

Priority Applications (no., kind, date): RU 1998122575 A 19981215

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
RU 2138117	C1	RU	0	0	

...11 and to other input, trough switch 12. Newly introduced in amplifier are low-value **resistor 8 connected** in series with **load 3, comparator** 16 whose inputs are **connected** to **resistor** 8, two OR gates 13, 14, and NOT gate 15. Depending on direction of load...

10/3,K/2 (Item 2 from file: 350) **Links**
Derwent WPIX

0002557310
WPI Acc no: 1982-K0917E/198230
Analog voltage-digital coder converter - has intermediate measuring converter producing current dependent on input signal to control bit position transistors in D-A converter
Patent Assignee: AS UKR CYBERNATICS (AUCY-R)
Inventor: BAGATSKII V A

Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
SU 869023	B	19810930	SU 2874150	A	19800125	198230	B

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
SU 869023	B	RU	4	2	

Alerting Abstract ...sign position current in the D-A converter (7), then a voltage drop at the **load resistor** (10) produces a signal at the **comparator** (3) output which maintains **connection** of the position current transistor (8) to an adding loop...

12/3,K/1 (Item 1 from file: 350) **Links**
Derwent WPIX

0002518206
WPI Acc no: 1982-E9863E/198217
DC voltage stabiliser - has two-threshold voltage comparator to enable automatic reset for any load resistance after fault clearance
Patent Assignee: OSADCHENKO V P (OSAD-I)
Inventor: OSADCHENKO V P; SHEPEL N G

Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
SU 847306	B	19810718	SU 2842053	A	19791113	198217	B

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
SU 847306	B	RU	3		

...
has two-threshold voltage comparator to enable automatic reset for any load resistance after fault clearance

14/3,K/1 (Item 1 from file: 350) Links
Derwent WPIX

0011023999 *Drawing available*
WPI Acc no: 2001-649781/200175
XRPX Acc No: N2001-485707
Load impedance detecting device for audio amplifiers, has digital circuit with two comparators to determine whether output current and voltage of amplifier is higher/lower than threshold value and reference voltage
Patent Assignee: STMICROELECTRONICS SRL (SGSA)
Inventor: CHIOZZI G; STORTI S

Patent Family (4 patents, 26 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
EP 1118865	A1	20010725	EP 2000830027	A	20000120	200175	B
US 20020093340	A1	20020718	US 2001760006	A	20010111	200254	E
			US 2001938747	A	20010823		
US 20030122549	A1	20030703	US 2001760006	A	20010111	200345	E
			US 2001938747	A	20010823		
			US 2002270023	A	20021010		
US 6812715	B2	20041102	US 2001760006	A	20010111	200472	E
			US 2001938747	A	20010823		
			US 2002270023	A	20021010		

Priority Applications (no., kind, date): EP 2000830027 A 20000120

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
EP 1118865	A1	EN	11	3		
Regional Designated States,Original	AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI					
US 20020093340	A1	EN			Continuation of application	US 2001760006
US 20030122549	A1	EN			Continuation of application	US 2001760006
					Continuation of application	US 2001938747
US 6812715	B2	EN			Continuation of application	US 2001760006
					Continuation of application	US 2001938747

...respectively determine whether the output current and voltage of amplifier is higher/lower than the **threshold value** and reference **voltage**. Flip-flops (11,14) respectively store the output of the two comparators.

17/3,K/1 (Item 1 from file: 347) Links
JAPIO

07975446 **Image available**
COMPARATOR CIRCUIT

Pub. No.: 2004-088205 [JP 2004088205 A]
Published: March 18, 2004 (20040318)
Inventor: MATSUI TAKAO

NAKAJIMA AKIO
FURUTA KOICHI
Applicant: SHIRINKUSU KK
SHARP CORP
Application No.: 2002-243270 [JP 2002243270]
Filed: August 23, 2002 (20020823)
International Class: **H03K-005/08**; H03F-003/45

ABSTRACT
...v1, v2; and an emitter follower circuit 3 applying positive feedback to the differential amplifier **2** and extracting **comparator** output voltages v5, v6. **Load resistors** R5, R6 of the differential amplifier 2 are connected to emitters of transistors Q3, Q4...

17/3,K/2 (Item 2 from file: 347) **Links**
JAPIO

04038187 **Image available**
COMPARATOR CIRCUIT

Pub. No.: 05-029887 [JP 5029887 A]
Published: February 05, 1993 (19930205)
Inventor: KOMORI TOMOHIRO
TANUMA JIRO
AKUTSU NAOJI
UCHIDA TAKAO
Applicant: OKI ELECTRIC IND CO LTD [000029] (A Japanese Company or Corporation), JP (Japan)
Application No.: 03-182609 [JP 91182609]
Filed: July 23, 1991 (19910723)
Journal: Section: E, Section No. 1381, Vol. 17, No. 313, Pg. 121, June 15, 1993 (19930615)
International Class: **H03K-003/023**; G01R-019/165

ABSTRACT
...is fed back to a base of a TR Q(sub 1). Let an output **load resistor** of the **comparator circuit** be R(sub **3**), an input **resistor** of an inverting input be R(sub 2) and a current amplification factor of the...

17/3,K/3 (Item 3 from file: 347) **Links**
JAPIO

03436621 **Image available**
COMPARING CIRCUIT

Pub. No.: 03-099521 [JP 3099521 A]
Published: April 24, 1991 (19910424)
Inventor: YANAGASE AKIO
Applicant: KYOEI SANGYO KK [325628] (A Japanese Company or Corporation), JP (Japan)
MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
Application No.: 01-236283 [JP 89236283]
Filed: September 12, 1989 (19890912)
Journal: Section: E, Section No. 1091, Vol. 15, No. 284, Pg. 133, July 18, 1991 (19910718)
International Class: H03M-001/36; **H03K-005/08**

ABSTRACT
...the offset of partial comparators exceeds the resolution, the bias current I(sub 1) of **two comparators** flows to a **load resistance** R(sub **3**) in the **comparator** interposed between these partial comparators, and voltage drop of 2XI(sub 1)XR(sub 3 ...

17/3,K/4 (Item 4 from file: 347) **Links**
JAPIO

02280019 **Image available**

COMPARATOR

Pub. No.: 62-196919 [JP 62196919 A]
Published: August 31, 1987 (19870831)
Inventor: KUSAMA NOBORU
Applicant: NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
Application No.: 61-039414 [JP 8639414]
Filed: February 25, 1986 (19860225)
Journal: Section: E, Section No. 582, Vol. 12, No. 49, Pg. 82, February 13, 1988 (19880213)
International Class: H03K-005/02; H03K-003/02; H03K-003/286

ABSTRACT
...highly accurate working of a comparator even in a high-speed action mode by cascading **comparators** at **plural** stages to set the **load resistance** of the comparator of the 1st stage at the input side at <=2/3 load...

17/3/5 (Item 1 from file: 350) **Links**
Derwent WPIX

0004307311 *Drawing available*
WPI Acc no: 1988-035630/198805
XRPX Acc No: N1988-026838
Band limited channel signal time intervals restorer - has input interfaced to relative averaging unit forming difference signal for comparator to obtain signals on zero-transition
Patent Assignee: KOZUBOV V N (KOZU-I)
Inventor: KOZUBOV V N

Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
SU 1320883	A	19870630	SU 3853145	A	19850206	198805	B

Priority Applications (no., kind, date): SU 3853145 A 19850206

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
SU 1320883	A	RU	6	4	

19/3,K/1 (Item 1 from file: 347) **Links**
JAPIO

05782845 **Image available**
POWER SUPPLY EQUIPMENT

Pub. No.: 10-065945 [JP 10065945 A]
Published: March 06, 1998 (19980306)
Inventor: OSAWA KATSUMI
Applicant: SONY CORP [000218] (A Japanese Company or Corporation), JP (Japan)
Application No.: 08-215783 [JP 96215783]
Filed: August 15, 1996 (19960815)

ABSTRACT
...DC current for load resistor sensing is supplied to a camera device 30 via a **resistor** R2 and a diode D1 and a **comparator** 3 supplies a level signal denoting a **load resistor** RL is a prescribed value or over to a port P1 of the microcomputer 8...

19/3,K/2 (Item 2 from file: 347) **Links**
JAPIO

05432084 **Image available**
POWER SUPPLY

Pub. No.: 09-046884 [JP 9046884 A]
Published: February 14, 1997 (19970214)
Inventor: TAKAHASHI YOSHIO
Applicant: SONY CORP [000218] (A Japanese Company or Corporation), JP (Japan)
Application No.: 07-192727 [JP 95192727]
Filed: July 28, 1995 (19950728)

ABSTRACT
...SOLUTION: A means for detecting **load impedance**, comprising a **comparator 3**, a reference **resistor** R, a variable resistor VR and a diode D1, is placed between a power supply...

19/3,K/3 (Item 3 from file: 347) **Links**
JAPIO

05322666 **Image available**
PHOTO-INTERRUPTER DEVICE

Pub. No.: 08-278166 [JP 8278166 A]
Published: October 22, 1996 (19961022)
Inventor: ODAJIMA SHIN
NUNOKAWA HIROYUKI
Applicant: COPAL CO LTD [000122] (A Japanese Company or Corporation), JP (Japan)
Application No.: 07-100687 [JP 95100687]
Filed: March 31, 1995 (19950331)

ABSTRACT
...movable slit, outputting a photoelectric current IC conformed to a light receiving quantity through a **load resistor** R. The **comparator 3** is equipped with a plus-minus input terminal and an output terminal. This plus-minus...

19/3,K/4 (Item 4 from file: 347) **Links**
JAPIO

03130629 **Image available**
BATTERY SAVING DEVICE

Pub. No.: 02-106129 [JP 2106129 A]
Published: April 18, 1990 (19900418)
Inventor: OSAWA TOMOYOSHI
OKANOUE KAZUHIRO
FURUYA YUKIAMI
NAGATA YOSHIAKI
KANAI TOSHIHITO
HAYAKAWA FUMIYASU
Applicant: NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
Application No.: 63-256183 [JP 88256183]
Filed: October 11, 1988 (19881011)
Journal: Section: E, Section No. 950, Vol. 14, No. 320, Pg. 127, July 10, 1990 (19900710)

ABSTRACT
...with the electrical appliance 5 can be predicted based on the ratio between the inner **resistance** and the **load** and the voltage **comparator 3** compares the battery voltage with a reference voltage being held therein. If a discrimination circuit...

19/3,K/5 (Item 5 from file: 347) **Links**
JAPIO

01806001 **Image available**
TEMPERATURE CONTROL DEVICE

Pub. No.: 61-020101 [JP 61020101 A]
Published: January 28, 1986 (19860128)
Inventor: OGINO TSUYOSHI
Applicant: MATSUSHITA REFRIG CO [000448] (A Japanese Company or Corporation), JP (Japan)
Application No.: 59-140887 [JP 84140887]
Filed: July 06, 1984 (19840706)
Journal: Section: P, Section No. 468, Vol. 10, No. 169, Pg. 17, June 14, 1986 (19860614)

ABSTRACT
...CONSTITUTION: A temperature control device is constituted of a temperature sensitive **resistor** element 1, a **comparator 3**, a **load** 8, etc. In said device, a diode 10 of which anode side is connected to...

19/3,K/6 (Item 6 from file: 347) **Links**
JAPIO

00594717 **Image available**
INVERTER UNIT WITH OPERATION STABILIZING UNIT

Pub. No.: 55-082317 [JP 55082317 A]
Published: June 21, 1980 (19800621)
Inventor: OKUBO HIDENORI
Applicant: FUJI ELECTRIC CO LTD [000523] (A Japanese Company or Corporation), JP (Japan)
Application No.: 53-154770 [JP 78154770]
Filed: December 15, 1978 (19781215)
Journal: Section: P, Section No. 27, Vol. 04, No. 131, Pg. 39, September 13, 1980 (19800913)

ABSTRACT
...CONSTITUTION: Current transformers 1 and **2, comparator** 4, relay 5 and false **load resistance** 6 are added to a parallel resonance-type high-frequency inverter constituted by SCR 7...

19/3,K/7 (Item 1 from file: 350) **Links**
Derwent WPIX

0008089390 *Drawing available*
WPI Acc no: 1997-186611/199717
XRPX Acc No: N1997-154117
Power supply operating mechanism for loads such as electronic component - includes relay which opens and closes power feed path between power supply circuit and load circuit
Patent Assignee: SONY CORP (SONY)
Inventor: TAKAHASHI Y

Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
JP 9046884	A	19970214	JP 1995192727	A	19950728	199717	B

Priority Applications (no., kind, date): JP 1995192727 A 19950728

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
JP 9046884	A	JA	5	4	

Alerting Abstract ...The mechanism includes a power supply circuit (1) which supplies electric power to a **load** circuit (2). A **comparator** (3) clutches the **impedance** of the **load** circuit. One end of the comparator input terminal is connected to a criteria resistance (R ...

19/3,K/8 (Item 2 from file: 350) **Links**
Derwent WPIX

0007921758 *Drawing available*
WPI Acc no: 1997-009513/199701
XRPX Acc No: N1997-008711
Parallel A/D converter used in hard disk appts, digital VTR, optical disk - in which constant current from current source of signal line connected to slave comparator of lower order bit, is made higher than that of higher order bit
Patent Assignee: HITACHI CHO LSI ENG CO LTD (HISC); HITACHI CHO LSI ENG KK (HISC); HITACHI LTD (HITA); HITACHI SEISAKUSHO KK (HITA); HITACHI VLSI ENG CORP (HISC)
Inventor: IMAIZUMI E; IMAIZUMI S; KASAHARA M; MATSUURA T; OKAZAWA H; ONO K

Patent Family (6 patents, 4 countries).

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
JP 8279751	A	19961022	JP 199619660	A	19960206	199701	B
TW 295746	A	19970111	TW 1996101268	A	19960201	199717	E
US 5684486	A	19971104	US 1996595999	A	19960206	199750	E
JP 03273887	B	20020415	JP 199619660	A	19960206	200233	E
JP 3273887	B2	20020415	JP 199619660	A	19960206	200233	E
KR 387173	B	20030821	KR 19962674	A	19960205	200412	E

Priority Applications (no., kind, date): JP 199517810 A 19950206

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
JP 8279751	A	JA	10	8		
TW 295746	A	ZH				
US 5684486	A	EN	14	8		
JP 03273887	B	JA	10		Previously issued patent	JP 08279751
JP 3273887	B2	JA	10		Previously issued patent	JP 08279751
KR 387173	B	KO			Previously issued patent	KR 96032441

Original Publication Data by Authority

...
Original Abstracts:
from a non-inverted output or inverted output of each master comparator, a plurality of **constant** current **sources**, a plurality of load resistors and a **plurality of** slave comparators **for** outputting desired **digital** signals. The constant current value of one of the constant current sources coupled to a...

19/3,K/9 (Item 3 from file: 350) **Links**
Derwent WPIX

0007920463 *Drawing available*
WPI Acc no: 1997-008210/199701
XRPX Acc No: N1997-007430
Photo-interrupting device for optical encoder - has comparator that compares detection voltage and monitor voltage and forms output pulse which shows displacement of mobility slit from output terminal
Patent Assignee: COPAL CO LTD (COPB)
Inventor: NUNOKAWA H; ODAJIMA S

Patent Family (2 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
JP 8278166	A	19961022	JP 1995100687	A	19950331	199701	B
JP 3552785	B2	20040811	JP 1995100687	A	19950331	200453	E

Priority Applications (no., kind, date): JP 1995100687 A 19950331

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
JP 8278166	A	JA	5	7		
JP 3552785	B2	JA	8		Previously issued patent	JP 08278166

Alerting Abstract ...beam through a mobility slit (4), and responds to a light-receiving quantity through a **load resistance** (RP). A **comparator (3)** with positive and negative input terminals, is provided...

19/3,K/10 (Item 4 from file: 350) **Links**
Derwent WPIX

0005630756 *Drawing available*
WPI Acc no: 1991-240183/199133
XRPX Acc No: N1991-183180
Electrical inductance and resistance measuring circuit - measures parameters, with resistance shunted by large reactions, also measures inductance with low Q-value
Patent Assignee: DU PONT UK LTD (DUPO); UPONOR BV (UPON-N)
Inventor: PAGE R; REEVES A V; WILLIAMS P M

Patent Family (4 patents, 12 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
EP 441649	A	19910814	EP 1991301043	A	19910208	199133	B
EP 441649	A3	19920422	EP 1991301043	A	19910208	199329	E
EP 441649	B1	19950816	EP 1991301043	A	19910208	199537	E
DE 69112092	E	19950921	DE 69112092	A	19910208	199543	E
			EP 1991301043	A	19910208		

Priority Applications (no., kind, date): GB 19902811 A 19900208

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
EP 441649	A	EN				
Regional Designated States,Original	AT BE CH DE ES FR GB GR IT LI LU NL SE					

EP 441649	A3	EN				
EP 441649	B1	EN	10	3		
Regional Designated States,Original	AT BE CH DE DK ES FR GB GR IT LI LU NL SE					
DE 69112092	E	DE			Application	EP 1991301043
					Based on OPI patent	EP 441649

Alerting Abstract ...A differential amplifier and gate circuit(s) produce a signal which is indicative of the **load** inductance. A **second comparator circuit** produces a signal indicative of the **load resistance**. Additional circuitry may be added to produce a signal indicative of the load capacitance...

Original Publication Data by Authority

19/3,K/11 (Item 5 from file: 350) Links
Derwent WPIX

0005244074 *Drawing available*
WPI Acc no: 1990-237398/199031
XRPX Acc No: N1990-183959
Amplifying arrangement for automatic controls - has additional resistors connected between output of pre-amplifying stage and input of each arm of push-pull output stage
Patent Assignee: GRAVVA YU N (GRAV-I)
Inventor: GRAVVA Y U N; PAVLYUK A F

Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
SU 1517117	A	19891023	SU 4375949	A	19871208	199031	B

Priority Applications (no., kind, date): SU 4375949 A 19871208

Alerting Abstract ...power amplifier (1) consisting of preliminary amplifying stage (5), push-pull output stage (6) and **resistors** (10,11), pulse amplifier (**2**), **comparators** (3,4), LF filters (7,8), **load** (12), **resistors** (13,14), double polarity comparator (15) and regulated resistors (16,17...

19/3,K/12 (Item 6 from file: 350) Links
Derwent WPIX

0004462449
WPI Acc no: 1988-204398/198829
XRPX Acc No: N1988-155918
Electromagnetic relay contacts cleaness monitor - has first output of first comparator connected to first input of dual AND-OR- NOT-gate
Patent Assignee: GOLDBERG I M (GOLD-I)
Inventor: GOLDBERG I M; RAKHMANOV A Y A

Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
SU 1363322	A	19871230	SU 4072982	A	19860415	198829	B

Priority Applications (no., kind, date): SU 4072982 A 19860415

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
SU 1363322	A	RU	4	1	

Alerting Abstract ...device, including lead-outs for connection of the tested relay's windings, supply source, two **load resistors**, **two** scaling amplifiers, and **comparators** and control unit, is now modified to give better test and monitoring fidelity, and includes...

19/3,K/13 (Item 7 from file: 350) Links
Derwent WPIX

0004218640
WPI Acc no: 1987-334008/198747
XRPX Acc No: N1987-249957
Digital units diagnostic performance tester - has preliminary check by bipolar pulses from pulse shapers and load resistors to each pair of contacts of two-contact connector
Patent Assignee: IMPULS COMUTER COMB (IMPU-R)
Inventor: LAMANOV G I; LOSENKO A N

Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
SU 1305688	A	19870423	SU 3904241	A	19850603	198747	B

Priority Applications (no., kind, date): SU 3904241 A 19850603

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
SU 1305688	A	RU	6	4	

Alerting Abstract ...and to the permissive inputs of the first of two sets of pulse shapers. A **third** digit **comparator**, an additional comparator, **load resistors**, a pseudo-random code generator and an indicator are also added to check the contacts...

19/3,K/14 (Item 8 from file: 350) Links
Derwent WPIX

0002801203
WPI Acc no: 1983-849893/198351

XRPX Acc No: N1983-228266
Angular displacement transducers tester - has timing-pulse generator interval discriminator, OR-gate, blocking unit, trigger and blocking time shaper
Patent Assignee: DUDIN D N (DUDI-I)
Inventor: BORODIN P I; DUDIN D N; DYLDIN S N

Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
SU 1002836	A	19830307	SU 3333628	A	19810826	198351	B

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
SU 1002836	A	RU	4	1	

Alerting Abstract ...of one of the angular displacement transducers (1-3), interconnected through converters (4-6) and **load resistors** (13-15) is disrupted, the corresponding **two** of the **three comparators** (7-9) will operate, thus tripping AND-gates (11, 10, 12) for transducers (1, 2...

19/3,K/15 (Item 9 from file: 350) **Links**
Derwent WPIX

0001994327
WPI Acc no: 1980-C4833C/198011
Smoothing filter for relay protection - uses comparator and timing for peak switching sequence capacitor charge, discharge to give fast response and ensured level of filtering
Patent Assignee: RIGA LATVENERGO (RILA-R)
Inventor: ARONSON V N; MYAGKOV A A

Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
SU 672575	A	19790705	SU 2566308	A	19780106	198011	B

Alerting Abstract ...output diagonal of which is applied to a series-connected diode (3), repeater (7), and **load resistor** (6). Across diode (3) is **comparator** (4) feeding through timer (5) to wiper of switch (2), which with capacitor (1) shunts...

19/3,K/16 (Item 10 from file: 350) **Links**
Derwent WPIX

0001832883
WPI Acc no: 1979-H8602B/197937
Three-phase system max. current square wave pulse shaper - has first OR-gate connected to semiconductor type interrupter and second OR-gate to rectifier bridge

Patent Assignee: NOVCH POLY (NCPO)
Inventor: ALLILUEV V A; ZASYPKIN A S

Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
SU 636549	A	19781210	SU 2495159	A	19770608	197937	B

Alerting Abstract ...Appts. includes current transformer, **load resistors**, rectifier bridge with plain capacitors, **two** OR-gates and **comparator**.

22/3,K/1 (Item 1 from file: 347) **Links**
JAPIO

08360131 **Image available**
SEMICONDUCTOR STORAGE DEVICE

Pub. No.: 2005-108391 [JP 2005108391 A]
Published: April 21, 2005 (20050421)
Inventor: TAKANO HIROSHI
Applicant: SANYO ELECTRIC CO LTD
Application No.: 2003-344467 [JP 2003344467]
Filed: October 02, 2003 (20031002)

ABSTRACT
...a bit line BL and comprising a ferroelectric capacitor 3 having hysteresis characteristics; and a **chopper comparator 2 connected** to the bit line BL and reading out data stored in the memory cell 1...

22/3,K/2 (Item 2 from file: 347) **Links**
JAPIO

06399179 **Image available**
PRECEDING VALUE DIFFERENCE COMPARATOR

Pub. No.: 11-340832 [JP 11340832 A]
Published: December 10, 1999 (19991210)
Inventor: ARISAKA KATSUMI
Applicant: CANON INC
Application No.: 10-150003 [JP 98150003]
Filed: May 29, 1998 (19980529)

ABSTRACT

PROBLEM TO BE SOLVED: To reduce comparison error and comparison redundant times by **connecting plural chopper** type **comparator** inputs, whose comparison timings are different in parallel, holding the compared outputs of the chopper...

22/3,K/3 (Item 1 from file: 350) **Links**
Derwent WPIX

0014973711 *Drawing available*
WPI Acc no: 2005-321544/200533
XRPX Acc No: N2005-262973

Semiconductor memory device e.g. ferroelectric memory, has chopper comparator for reading data stored in ferroelectric capacitor and supplying prescribed energy that changes storage state of capacitor from initial state
Patent Assignee: SANYO ELECTRIC CO LTD (SAOL)
Inventor: TAKANO H; TAKANO Y

Patent Family (3 patents, 2 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 20050073870	A1	20050407	US 2004947367	A	20040923	200533	B
JP 2005108391	A	20050421	JP 2003344467	A	20031002	200533	E
US 7133305	B2	20061107	US 2004947367	A	20040923	200673	E

Priority Applications (no., kind, date): JP 2003344467 A 20031002; US 2004947367 A 20040923

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
US 20050073870	A1	EN	11	6	
JP 2005108391	A	JA	16		

...NOVELTY - The device has a **chopper comparator (2) connected** to a data read line for reading data stored in a ferroelectric capacitor (3). The...

22/3,K/4 (Item 2 from file: 350) **Links**
Derwent WPIX

0009278172 *Drawing available*
WPI Acc no: 1999-207380/199918
XRPX Acc No: N1999-152795
Analogue/Digital convertor circuit
Patent Assignee: FUJITSU LTD (FUIT); FUJITSU VLSI LTD (FUIV)
Inventor: ANDO K; ANDOU K; TSUKAMOTO S

Patent Family (6 patents, 5 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
FR 2767984	A1	19990305	FR 19984614	A	19980414	199918	B
JP 11145832	A	19990528	JP 1998106645	A	19980416	199932	E
KR 1999029182	A	19990426	KR 199816250	A	19980507	200028	E
US 6218975	B1	20010417	US 199846679	A	19980324	200123	E
TW 419904	A	20010121	TW 1998105081	A	19980403	200138	E
KR 279878	B	20010201	KR 199816250	A	19980507	200211	E

Priority Applications (no., kind, date): JP 1997237324 A 19970902

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
FR 2767984	A1	FR	64	30		
JP 11145832	A	JA	22			
KR 1999029182	A	KO		30		
TW 419904	A	ZH				
KR 279878	B	KO			Previously issued patent	KR 99029182

Original Publication Data by Authority

...
Claims:
subsequent to the auto-zero operation; a controller circuit, coupled to the plurality of chopper **type** comparators, controlling **one** comparator **to** perform **the** auto-zero operation and the remaining comparators to perform the comparing operations, substantially simultaneously, the...

22/3,K/5 (Item 3 from file: 350) **Links**
Derwent WPIX

0006721081 *Drawing available*
WPI Acc no: 1994-102899/199413
XRPX Acc No: N1994-080335
Data slicer with hold circuit - includes comparator and clamping circuit, with circuit having diode between comparator input and voltage supply, transistor and bias circuit
Patent Assignee: MOTOROLA INC (MOTI)
Inventor: MAIN; MAIN W E

Patent Family (7 patents, 6 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
EP 589164	A1	19940330	EP 1993111356	A	19930715	199413	B
JP 6196979	A	19940715	JP 1993250989	A	19930914	199433	E
US 5365120	A	19941115	US 1992947625	A	19920921	199445	E
SG 46252	A1	19980220	SG 19961636	A	19930715	199821	E
EP 589164	B1	19991006	EP 1993111356	A	19930715	199946	E
DE 69326662	E	19991111	DE 69326662	A	19930715	199954	E
			EP 1993111356	A	19930715		
JP 3152270	B2	20010403	JP 1993250989	A	19930914	200121	E

Priority Applications (no., kind, date): US 1992947625 A 19920921

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
EP 589164	A1	EN	7	3		
Regional Designated States,Original	DE FR GB					
JP 6196979	A	JA	6			
US 5365120	A	EN	6	3		
SG 46252	A1	EN				
EP 589164	B1	EN				
Regional Designated States,Original	DE FR GB					
DE 69326662	E	DE			Application	EP 1993111356
					Based on OPI patent	EP 589164
JP 3152270	B2	JA	6		Previously issued patent	JP 06196979

Original Publication Data by Authority

...
Claims:
input of said comparator being coupled to the input of the data slicer, said second **input** of **said** comparator being coupled **to** receive **a** bias voltage, said output of said comparator being coupled to the output of the data... ... being coupled to receive a bias voltage (VB), said output of said comparator (10) being **coupled** to the **output** (20) of the **data** slicer (5); **and** clamping means (12) coupled to said first input of said comparator (10), said clamping means ... being coupled to the output of the data slicer; and clamping means coupled to said **first** input **of** said comparator, said **clamping** including: **(a)** a first transistor having a collector, a base and an emitter, said collector of said f...

23/3,K/1 (Item 1 from file: 350) **Links**
Derwent WPIX

0014772816 *Drawing available*
WPI Acc no: 2005-120481/200513
XRPX Acc No: N2005-103925
Data slicer for use in data transmission system, has three comparator circuits, each establishing respective threshold, where two of comparator circuits have symmetrical offsets and include load resistor that has center tap
Patent Assignee: BROWN W W (BROW-I)
Inventor: **BROWN W W**

Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 20050008099	A1	20050113	US 2003616214	A	20030708	200513	B

Priority Applications (no., kind, date): US 2003616214 A 20030708

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
US 20050008099	A1	EN	5	1	

Inventor: **BROWN W W**

...NOVELTY - The **slicer** (12) has **three comparator circuits**, each circuit establishing a respective threshold. Each of the comparator circuits has an offset. Two...

Original Publication Data by Authority

Inventor name & address:
Brown, William W...
Original Abstracts:
A PAM-4 data slicer includes first, second, **and** third comparators **which** provide **first, second,** and third thresholds, **respectively**. Each of the comparators has an offset. The first and third comparators have an offset...

[File 348] **EUROPEAN PATENTS** 1978-2007/ 200708
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**File 348: For important information about IPCR/8 and forthcoming changes to the IC= index, see HELP NEWSIPCR.*

[File 349] **PCT FULLTEXT** 1979-2007/UB=20070315UT=20070308
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**File 349: For important information about IPCR/8 and forthcoming changes to the IC= index, see HELP NEWSIPCR.*

```
Set     Items   Description
S1      56985   S COMPARATOR?? OR COMPARATOR??()CIRCUIT???
S2          0   S (PAM()4 OR (FET OR FIELD()EFFECT()TRANSISTOR??)(3N)CMOS)(3N)S1
S3      18043   S (PLURAL? OR MULTI OR MULTIPLE OR MANY SEVERAL OR MORE(1N)ONE OR TWO
OR 2 OR SECOND OR NUMEROUS OR THIRD OR THREE OR 3 OR PAIR??)(3N)(S1 OR S2)
S4         11   S LOAD(3N)(RESISTANCE OR RESISTOR?? OR IMPEDANCE)(3N)S3
S5          0   S (CENTER()TAP? OR NODE?? OR SLICE??)(3N)S4
S6          2   S (INTERCONNECT?? OR COUPL? OR WIRE?? OR CONNECT??? OR ATTACH???? OR
LINK??? OR JOIN??? OR INTEGA??? OR OPERATIVE?)(3N)(S4 OR S5)
S7      64405   S VOLT???(3N)(OFFSET???? OR OFF()SET???? OR THRESHOLD OR FACTORS OR
VALUE OR MAX OR MAXIMUM OR NUMBER)
S8        410   S AU=(BROWN, W? OR BROWN W?)
S9          8   S S4 NOT AD=20030708:20070322/PR
S10       339   S S3(3N)S7
S11         0   S S10(3N)(LOAD(3N)(RESISTANCE OR RESISTOR?? OR IMPEDANCE))
S12         2   S S10(20N)(LOAD(3N)(RESISTANCE OR RESISTOR?? OR IMPEDANCE))
S13         2   S S12 NOT (S6 OR S9)
S14         0   S S10 AND S8
S15        24   S S7(3N)SYMMETRIC(3N)(OFFSET? OR OFF()SET?)
S16         0   S S15(40N)S2
S17         0   S S15 AND S2
S18         0   S S15 AND (IC=H04L? OR IC=HO3K?)
S19        23   S S15 NOT AD=20030708:20070322/PR
S20         7   S S19 AND (LINEARIZED(1N)AMPLIFIER OR SYMMETRIC(1N)AMPLIFIER OR
HALL()DEVICE OR INTEGRATED(2N)FILTER)
```

6/3K/1 (Item 1 from file: 348) Links
EUROPEAN PATENTS
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00269794
Daisy chain collision detection circuit.
Kollisionserkennungsschaltung fur daisy chain.
Circuit de detection de collision pour daisy chain.

Patent Assignee:

- **ADVANCED MICRO DEVICES, INC.**; (328120)
  901 Thompson Place P.O. Box 3453; Sunnyvale, CA 94088; (US)
  (applicant designated states: AT;BE;CH;DE;ES;FR;GB;GR;IT;LI;LU;NL;SE)

Inventor:

- **Duley, Raymond Stephen**
  704 Leisurewoods; Buda Texas 78610; (US)
- **Forth, Leslie**
  13200 Viento del Sur; Manchaca Texas; (US)

Legal Representative:

• **Barnard, Eric Edward et al (28021)**
BROOKES & MARTIN High Holborn House 52/54 High Holborn; London WC1V 6SE; (GB)

	Country	Number	Kind	Date	
Patent	EP	271179	A2	19880615	(Basic)
	EP	271179	A3	19900404	
	EP	271179	B1	19930901	
Application	EP	87307250		19870817	
Priorities	US	941238		19861212	

Designated States:
AT; BE; CH; DE; ES; FR; GB; GR; IT; LI;
LU; NL; SE;

International Patent Class (V7): H04L-012/28; ; **Abstract Word Count:** 128

Type	Pub. Date	Kind	Text

Publication: English
Procedural: English
Application: English

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	1489
CLAIMS B	(German)	EPBBF1	1240
CLAIMS B	(French)	EPBBF1	1677
SPEC B	(English)	EPBBF1	3992
Total Word Count (Document A) 0			
Total Word Count (Document B) 8398			
Total Word Count (All Documents) 8398			

Specification: ...polarity power source. The voltage comparator U2 has an open collector output which requires an **external resistor load**. A **third** voltage divider formed of series-**connected resistors R5** and R6 is provided to serve as the external load. The junction of the resistors...

6/3K/2 (Item 1 from file: 349) **Links**
PCT FULLTEXT

01116677
ADVANCED DIGITAL ANTENNA MODULE
MODULE D'ANTENNE NUMERIQUE EVOLUE

Patent Applicant/Patent Assignee:

• **RAYTHEON COMPANY**; 2000 E. El Segundo Boulevard, P.O. Box 902 (E4/N119), El Segundo, CA 90245-0902 US; US(Residence); US(Nationality)

Legal Representative:

• **ALKOV Leonard A(et al)(agent)**
c/o RAYTHEON COMPANY, 2000 E. El Segundo Boulevard, P.O. Box 902 (E4/N119), El Segundo, CA 90245-0902; US;

	Country	Number	Kind	Date
Patent	WO	200438922	A2-A3	20040506
Application	WO	2003US33748		20031023
Priorities	US	2002280680		20021025

Designated States: (All protection types applied unless otherwise stated - for applications 2004+)

[EP] AT; BE; BG; CH; CY; CZ; DE; DK; EE; ES;
FI; FR; GB; GR; HU; IE; IT; LU; MC; NL;
PT; RO; SE; SI; SK; TR;

Publication Language: English
Filing Language: English
Fulltext word count: 5576

Detailed Description:

...to VNS by R7 and R8, respectively. The bases of Q108, Q58, and Q59 are **connected** to VBIPI.

The **comparator** 62 has **3** features that enhance performance. The **load resistors**, 5 pairs R25 (active mode) and R26 and pairs R24 (active mode) and R49 are ..

9/3K/1 (Item 1 from file: 348) Links
EUROPEAN PATENTS

01143321
Overcurrent sensing circuit and self adjusting protection
Uberstromsensorschaltung und sich selbsteinstellender Schutz
Circuit de detection de surintensite et protection a reglage automatique

Patent Assignee:

- **Intersil Corporation**; (2832870)
  2401 Palm Bay Road, N.E.; Palm Bay, Florida 32905; (US)
  (Applicant designated States: all)

Inventor:

- **Pullen, Stuart**
  3802 Kelford Street; Raleigh, NC 27606; (US)

Legal Representative:

- **van Berlyn, Ronald Gilbert (37011)**
  23, Centre Heights; London NW3 6JG; (GB)

	Country	Number	Kind	Date	
Patent	EP	998030	A1	20000503	(Basic)
Application	EP	99120865		19991026	
Priorities	US	183453		19981030	

Designated States:
AT; BE; CH; CY; DE; DK; ES; FI; FR; GB;
GR; IE; IT; LI; LU; MC; NL; PT; SE;

Extended Designated States:
AL; LT; LV; MK; RO; SI;

International Patent Class (V7): H03F-003/217; H03F-001/52; H03K-017/082**Abstract Word Count:** 127
NOTE: 1
NOTE: Figure number on first page: 1

Type	Pub. Date	Kind	Text
Publication: English			
Procedural: English			
Application: English			

Available Text	Language	Update	Word Count

CLAIMS A	(English)	200018	395
SPEC A	(English)	200018	2746
Total Word Count (Document A) 3141			
Total Word Count (Document B) 0			
Total Word Count (All Documents) 3141			

Specification: ...proportional to the load impedance. The first comparator 303 detects a short circuit (almost zero **load impedance**); the **second comparator** detects a low **impedance** condition (one to two ohms).

The first comparator 303 has a short circuit reference voltage...

9/3K/2 (Item 2 from file: 348) Links
EUROPEAN PATENTS

00395357
Amplifier arrangement with saturation detection.
Verstarkerschaltung mit Sattigungsdetektion.
Circuit amplificateur a detection de saturation.

Patent Assignee:

- **N.V. Philips' Gloeilampenfabrieken**; (200769)
  Groenewoudseweg 1; NL-5621 BA Eindhoven; (NL)
  (applicant designated states: DE;FR;GB;IT;NL)

Inventor:

- **Van den Bungelaar, Martinus Joseph**
  c/o INT. OCTROOIBUREAU B.V., Prof. Holstlaan 6; NL-5656 AA Eindhoven; (NL)

Legal Representative:

- **Peters, Rudolf Johannes et al (49051)**
  INTERNATIONAAL OCTROOIBUREAU B.V. Prof. Holstlaan 6; NL-5656 AA Eindhoven; (NL)

	Country	Number	Kind	Date	
Patent	EP	385547	A1	19900905	(Basic)
Application	EP	90200443		19900226	
Priorities	NL	89507		19890302	

Designated States:
DE; FR; GB; IT; NL;

International Patent Class (V7): H03F-001/32; H03F-001/34; **Abstract Word Count:** 191

Type	Pub. Date	Kind	Text
Publication: English			
Procedural: English			
Application: English			

Available Text	Language	Update	Word Count
CLAIMS A	(English)		560
SPEC A	(English)		4127
Total Word Count (Document A) 4687			
Total Word Count (Document B) 0			
Total Word Count (All Documents) 4687			

Specification: ...sub(t)))/(R3 + R4). This current I(sub(D)) like the output signal of the **comparator** 16 in Fig. 3 is independent of the **load impedance** Z(sub(L)) at the output terminal 4 of the amplifier arrangement.

If saturation of...

9/3K/3 (Item 3 from file: 348) **Links**
EUROPEAN PATENTS

00326439
Active overvoltage control for inductive load driving.
Aktive Uberspannungsuberwachung fur den Betrieb einer induktiven Last.
Controle actif de surtension pour l'operation d'une charge a induction.

Patent Assignee:

- **SGS-THOMSON MICROELECTRONICS s.r.l.**; (1014060)
  Via C. Olivetti, 2; I-20041 Agrate Brianza Milano; (IT)
  (applicant designated states: DE;FR;GB)

Inventor:

- **Gariboldi, Roberto**
  Via F. Baracca, 6/3; I-20084 Lacchiarella; (IT)
- **Gola, Alberto**
  Via Eseguiti, 22 bis; I-27043 Broni; (IT)

Legal Representative:

- **Pellegri, Alberto et al (45781)**
  c/o Societa Italiana Brevetti S.p.A. Via Puccini, 7; I-21100 Varese; (IT)

	Country	Number	Kind	Date	
Patent	EP	311576	A2	19890412	(Basic)
	EP	311576	A3	19910109	
	EP	311576	B1	19940223	
Application	EP	88830401		19881004	
Priorities	IT	8783662		19871009	

Designated States:
DE; FR; GB;

International Patent Class (V7): H02H-009/04; ; **Abstract Word Count:** 113

Type	Pub. Date	Kind	Text

Publication: English
Procedural: English
Application: Italian

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	309
CLAIMS B	(German)	EPBBF1	288
CLAIMS B	(French)	EPBBF1	346
SPEC B	(English)	EPBBF1	1601
Total Word Count (Document A) 0			
Total Word Count (Document B) 2544			
Total Word Count (All Documents) 2544			

Specification: ...the voltage divider through which the reference voltage is sensed. Such a buffer element is **formed by** the **two** transistor Q1 **and Q2** and by the respective **load resistors** R6 and R5.

The comparator circuit operates in the following way. When the voltage V1...

9/3K/4 (Item 4 from file: 348) Links
EUROPEAN PATENTS

00269794
Daisy chain collision detection circuit.
Kollisionserkennungsschaltung fur daisy chain.
Circuit de detection de collision pour daisy chain.

Patent Assignee:

- **ADVANCED MICRO DEVICES, INC.**; (328120)
  901 Thompson Place P.O. Box 3453; Sunnyvale, CA 94088; (US)
  (applicant designated states: AT;BE;CH;DE;ES;FR;GB;GR;IT;LI;LU;NL;SE)

Inventor:

- **Duley, Raymond Stephen**
  704 Leisurewoods; Buda Texas 78610; (US)
- **Forth, Leslie**
  13200 Viento del Sur; Manchaca Texas; (US)

Legal Representative:

- **Barnard, Eric Edward et al (28021)**
  BROOKES & MARTIN High Holborn House 52/54 High Holborn; London WC1V 6SE; (GB)

	Country	Number	Kind	Date	
Patent	EP	271179	A2	19880615	(Basic)
	EP	271179	A3	19900404	
	EP	271179	B1	19930901	
Application	EP	87307250		19870817	
Priorities	US	941238		19861212	

Designated States:
AT; BE; CH; DE; ES; FR; GB; GR; IT; LI;
LU; NL; SE;

International Patent Class (V7): H04L-012/28; ; **Abstract Word Count:** 128

Type	Pub. Date	Kind	Text

Publication: English
Procedural: English
Application: English

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	1489
CLAIMS B	(German)	EPBBF1	1240
CLAIMS B	(French)	EPBBF1	1677
SPEC B	(English)	EPBBF1	3992
Total Word Count (Document A) 0			
Total Word Count (Document B) 8398			
Total Word Count (All Documents) 8398			

Specification: ...polarity power source. The voltage comparator U2 has an open collector output which requires an **external resistor load**. A **third** voltage divider formed of series-connected **resistors R5** and R6 is provided to serve as the external load. The junction of the resistors...

9/3K/5 (Item 1 from file: 349) Links
PCT FULLTEXT

01194109
POWER CONTROL FOR AN ELECTRICALLY POWERED WATER TREATMENT APPARATUS
REGLAGE DE PUISSANCE POUR UN APPAREIL ELECTRIQUE DE TRAITEMENT DE L'EAU

Patent Applicant/Patent Assignee:

- **W2W LLC**; 150 Commerce Road, Carlstadt, NJ 07072
  US; US(Residence); US(Nationality)
  (For all designated states except: US)
- **LIVSHITS David**; Haatzmaut Street 40-24, 77452 Ashdod
  IL; IL(Residence); IL(Nationality)
  (Designated only for: US)

Patent Applicant/Inventor:

- **LIVSHITS David**
  Haatzmaut Street 40-24, 77452 Ashdod; IL; IL(Residence); IL(Nationality); (Designated only for: US)

Legal Representative:

- **RONALD Abramson(agent)**
  Hughes Hubbard & Reed LLP, One Battery Park Plaza, New York, NY 10004-1482; US;

	Country	Number	Kind	Date
Patent	WO	200501164	A1	20050106
Application	WO	2004US16628		20040621
Priorities	US	2003480359		20030620

Designated States: (All protection types applied unless otherwise stated - for applications 2004+)
AE; AG; AL; AM; AT; AU; AZ; BA; BB; BG;
BR; BW; BY; BZ; CA; CH; CN; CO; CR; CU;
CZ; DE; DK; DM; DZ; EC; EE; EG; ES; FI;
GB; GD; GE; GH; GM; HR; HU; ID; IL; IN;
IS; JP; KE; KG; KP; KR; KZ; LC; LK; LR;
LS; LT; LU; LV; MA; MD; MG; MK; MN; MW;
MX; MZ; NA; NI; NO; NZ; OM; PG; PH; PL;
PT; RO; RU; SC; SD; SE; SG; SK; SL; SY;
TJ; TM; TN; TR; TT; TZ; UA; UG; US; UZ;
VC; VN; YU; ZA; ZM; ZW;

[EP] AT; BE; BG; CH; CY; CZ; DE; DK; EE; ES;
FI; FR; GB; GR; HU; IE; IT; LU; MC; NL;
PL; PT; RO; SE; SI; SK; TR;

[OA] BF; BJ; CF; CG; CI; CM; GA; GN; GQ; GW;
ML; MR; NE; SN; TD; TG;

[AP] BW; GH; GM; KE; LS; MW; MZ; NA; SD; SL;
SZ; TZ; UG; ZM; ZW;

[EA] AM; AZ; BY; KG; KZ; MD; RU; TJ; TM;

Publication Language: English
Filing Language: English
Fulltext word count: 19979

Detailed Description:

...and tolerances of each of the separate
components, input rectifier 1% high-frequency power converter 2% output rectifier Y, **comparator** 41, and **resistance** or **load** R,

of each of the voltage sensor/stabilizer (VS), and of the current sensor/stabilizer...

9/3K/6 (Item 2 from file: 349) Links
PCT FULLTEXT

01116677
ADVANCED DIGITAL ANTENNA MODULE
MODULE D'ANTENNE NUMERIQUE EVOLUE

Patent Applicant/Patent Assignee:

- **RAYTHEON COMPANY**; 2000 E. El Segundo Boulevard, P.O. Box 902 (E4/N119), El Segundo, CA 90245-0902 US; US(Residence); US(Nationality)

Legal Representative:

- **ALKOV Leonard A(et al)(agent)**
  c/o RAYTHEON COMPANY, 2000 E. El Segundo Boulevard, P.O. Box 902 (E4/N119), El Segundo, CA 90245-0902; US;

	Country	Number	Kind	Date
Patent	WO	200438922	A2-A3	20040506
Application	WO	2003US33748		20031023
Priorities	US	2002280680		20021025

Designated States: (All protection types applied unless otherwise stated - for applications 2004+)

[EP] AT; BE; BG; CH; CY; CZ; DE; DK; EE; ES;
FI; FR; GB; GR; HU; IE; IT; LU; MC; NL;
PT; RO; SE; SI; SK; TR;

Publication Language: English
Filing Language: English
Fulltext word count: 5576

Detailed Description:

...and R8, respectively. The bases of Q108, Q58, and Q59 are connected to VBIPI.

The **comparator** 62 has **3** features that enhance performance. The **load resistors**, 5 pairs R25 (active mode) and R26 and pairs R24 (active mode) and R49 are...

Claims:

...circuit (40) includes a
trimmable digital-to-analog converter (32).
7 The invention of Claim **3** wherein said **comparator** (62) includes:
split **load resistors**, pairs R25 (active mode) and R26 and pairs R24(active mode) and R49;latch pair...

9/3K/7 (Item 3 from file: 349) Links
PCT FULLTEXT

00987377

COMPARATOR WITH VERY FAST REGENERATION TIME CONSTANT
COMPARATEUR PRESENTANT UNE CONSTANTE DE TEMPS DE REGENERATION TRES RAPIDE

Patent Applicant/Patent Assignee:

- **HRL LABORATORIES LLC**; 3011 Malibu Canyon Road, Malibu, CA 90265-4799
  US; US(Residence); US(Nationality)
  (For all designated states except: US)
- **COSAND Albert E**; 6152 Chesebro Road, Agoura Hills, CA 91301
  US; US(Residence); US(Nationality)
  (Designated only for: US)

Patent Applicant/Inventor:

- **COSAND Albert E**
  6152 Chesebro Road, Agoura Hills, CA 91301; US; US(Residence); US(Nationality); (Designated only for: US)

Legal Representative:

- **BERG Richard P(et al)(agent)**
  Ladas & Parry, 5670 Wilshire Boulevard, Suite 2100, Los Angeles, CA 90036-5679; US;

	Country	Number	Kind	Date
Patent	WO	200317485	A2-A3	20030227
Application	WO	2002US25907		20020813
Priorities	US	2001931609		20010816

Designated States: (All protection types applied unless otherwise stated - for applications 2004+)

[EP] AT; BE; BG; CH; CY; CZ; DE; DK; EE; ES;
FI; FR; GB; GR; IE; IT; LU; MC; NL; PT;
SE; SK; TR;

[OA] BF; BJ; CF; CG; CI; CM; GA; GN; GQ; GW;
ML; MR; NE; SN; TD; TG;

[AP] GH; GM; KE; LS; MW; MZ; SD; SL; SZ; TZ;
UG; ZM; ZW;

[EA] AM; AZ; BY; KG; KZ; MD; RU; TJ; TM;

Publication Language: English
Filing Language: English
Fulltext word count: 7548

Claims:

...the load resistors and operating as cascode amplifier stages to couple the currents in the **load resistors** to the **comparator** output. 3. The **comparator** of claim 1 or 2, wherein the comparator output is a' voltage difference signal. 4...

9/3K/8 (Item 4 from file: 349) Links
PCT FULLTEXT

00170450
MONITORING CIRCUITS FOR ELECTRICAL LOADS, ESPECIALLY FOR MONITORING LAMPS

CIRCUITS DE CONTROLE POUR CHARGES ELECTRIQUES, EN PARTICULIER POUR LAMPES

Patent Applicant/Patent Assignee:

- **KING Gordon Alan;**
  ; ;

- **NIMMO George Ross;**
  ; ;

	Country	Number	Kind	Date
Patent	WO	9003900	A1	19900419
Application	WO	89GB1214		19891013
Priorities	GB	8824095		19881014

Designated States: (All protection types applied unless otherwise stated - for applications 2004+)

Publication Language: English
Filing Language:
Fulltext word count: 4745

Detailed Description:

...comparator input signal is a signal indicative
of the potential of a point between the **resistor** and the **load** and
the **second comparator** input signal is a reference signal
indicative of a first reference potential during cold monitoring .

13/3K/1 (Item 1 from file: 348) **Links**
EUROPEAN PATENTS

00846981
METHOD AND APPARATUS FOR PROTECTING A MONEY-HANDLING UNIT VULNERABLE TO LIQUID
VERFAHREN UND VORRICHTUNG ZUM SCHUTZ EINER DURCH FLUSSIGKEITEN VERLETZBAREN GELDVERARBEITUNGSVORRICHTUNG
PROCEDE ET APPAREIL DE PROTECTION D'UNE MACHINE A PIECES DE MONNAIE VULNERABLE AUX LIQUIDES

Patent Assignee:

- **MARS, INCORPORATED**; (255781)
  6885 Elm Street; McLean, Virginia 22101-3883; (US)
  (Proprietor designated states: all)

Inventor:

- **DILLON, Stephen, John**
  Dodds Cottage, Mariners Lane; Southend, Reading,RG7 6HU; (GB)

- **MIR, Andrew**
  3 The Crescent; Old Harlow Essex CM17 0HM; (GB)

Legal Representative:

- **Burke, Steven David et al (47741)**
  R.G.C. Jenkins & Co. 26 Caxton Street; London SW1H 0RJ; (GB)

	Country	Number	Kind	Date	
Patent	EP	867019	A1	19980930	(Basic)
	EP	867019	B1	20020320	

	WO	9709697		19970313	
Application	EP	96929442		19960906	
	WO	96GB2206		19960906	
Priorities	GB	9518649		19950907	

Designated States:
DE; ES; FR; GB; IT;

International Patent Class (V7): G07F-001/04
NOTE: No A-document published by EPO

Type	Pub. Date	Kind	Text

Publication: English
Procedural: English
Application: English

Available Text	Language	Update	Word Count
CLAIMS B	(English)	200212	1569
CLAIMS B	(German)	200212	1432
CLAIMS B	(French)	200212	1764
SPEC B	(English)	200212	6455
Total Word Count (Document A) 0			
Total Word Count (Document B) 11220			
Total Word Count (All Documents) 11220			

Specification: ...coupled in series across the power supply rails as a potential divider. The reference or **threshold voltage** for the **second comparator** is likewise set at input 94 by two further resistors R4 and R5. The sensor 80 is coupled to a **load resistor** R3 to form a potential divider giving a sensed voltage at node 96.

Under normal...

13/3K/2 (Item 1 from file: 349) **Links**
PCT FULLTEXT

00369369
METHOD AND APPARATUS FOR PROTECTING A MONEY-HANDLING UNIT VULNERABLE TO LIQUID
PROCEDE ET APPAREIL DE PROTECTION D'UNE MACHINE A PIECES DE MONNAIE VULNERABLE AUX LIQUIDES

Patent Applicant/Patent Assignee:

- **MARS INCORPORATED;**
  ; ;

- **DILLON Stephen John;**
  ; ;

- **MIR Andrew;**
  ; ;

	Country	Number	Kind	Date
Patent	WO	9709697	A1	19970313
Application	WO	96GB2206		19960906
Priorities	GB	9518649		19950907

Designated States: (All protection types applied unless otherwise stated - for applications 2004+)

Publication Language: English

Filing Language:
Fulltext word count: 8889

Detailed Description:

...coupled in series across the power supply rails as a potential divider. The reference or **threshold voltage** for the **second comparator** is likewise set at input 94 by two further resistors R4 and R5. The sensor 80 is coupled to a **load resistor** R3 to form a potential divider giving a sensed voltage at node 96.

Under normal...

20/3K/1 (Item 1 from file: 348) **Links**
EUROPEAN PATENTS

01203419
Disbtributed gain line driver amplifier
Leitungstreiberverstarker mit verteilter Verstarkung
Amplificateur d'attaque de ligne de gain distribue

Patent Assignee:

- **LUCENT TECHNOLOGIES INC.**; (2143720)
  600 Mountain Avenue; Murray Hill, New Jersey 07974-0636; (US)
  (Proprietor designated states: all)

Inventor:

- **Shulman, Dima David**
  10 Whitney Drive; Marlboro,New Jersey 07746; (US)

Legal Representative:

- **Williams, David John et al (86433)**
  Page White & Farrer, 54 Doughty Street; London WC1N 2LS; (GB)

	Country	Number	Kind	Date	
Patent	EP	1047184	A2	20001025	(Basic)
	EP	1047184	A3	20040331	
	EP	1047184	B1	20060531	
Application	EP	2000303265		20000418	
Priorities	US	299237		19990423	

Designated States:
DE; FR; GB;

Extended Designated States:
AL; LT; LV; MK; RO; SI;

International Patent Class (V7): H03F-001/18; H03F-003/60

IPC	Level	Value	Position	Status	Version	Action	Source	Office
H03F-0001/18	A	I	F	B	20060101	20000622	H	EP
H03F-0003/60	A	I	L	B	20060101	20000622	H	EP

Abstract Word Count: 267
NOTE: 3
NOTE: Figure number on first page: 3

Type	Pub. Date	Kind	Text

Publication: English

Procedural: English
Application: English

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200043	928
SPEC A	(English)	200043	2584
CLAIMS B	(English)	200622	1195
CLAIMS B	(German)	200622	1045
CLAIMS B	(French)	200622	1284
SPEC B	(English)	200622	2652
Total Word Count (Document A) 3513			
Total Word Count (Document B) 6176			
Total Word Count (All Documents) 9689			

Specification: ...stage of a prior known line driver amplifier 100. Amplifier 100 is a so-called **symmetrical amplifier** of a type well known in the art including two similar output stages. One amplifier... ...output voltage at output 404 relative to the voltage when transistors 402 and 403 are **symmetrical**. Thus, resulting in a desired **offset voltage** level, in accordance with the invention. Note that in practice, it is advantageous to have...

Specification: ...stage of a prior known line driver amplifier 100. Amplifier 100 is a so-called **symmetrical amplifier** of a type well known in the art including two similar output stages. One amplifier... ...output voltage at output 404 relative to the voltage when transistors 402 and 403 are **symmetrical**. Thus, resulting in a desired **offset voltage** level, in accordance with the invention. Note that in practice, it is advantageous to have...

Claims: ...connected in circuit with said first amplifier stage wherein said amplifier is arranged as a **symmetrical amplifier**.

3. The amplifier as defined in claim 2 wherein said second amplifier stage includes a...

Claims: ...circuit with said first amplifier stage (301) wherein said amplifier (300) is arranged as a **symmetrical amplifier**.

3. The amplifier as defined in claim 2 CHARACTERIZED IN THAT said second amplifier stage...

20/3K/2 (Item 2 from file: 348) **Links**
EUROPEAN PATENTS

00746758
Method for compensating the piezoresistive offset voltage in doubly connected Hall effect devices based on silicon
Verfahren zur Kompensation der piezoresistiver Offsetspannung in doppelverbundenen siliziumbasierenden Hall Effekt Elementen
Methode pour compenser la tension piezoresistive de decalage d'un dispositif a effet Hall a connection double a base de silicium

Patent Assignee:

- **Ramesh, G. Mani, Dr.**; (4266970)
  c/o Harvard University, Gordon McKay Laboratory of Applied Science, 9 Oxford Street; Cambridge, MA 2138; (US)
  (Proprietor designated states: all)

Inventor:

- **Mani, Ramesh G.**
  Forststrasse 91; 70176 Stuttgart; (DE)
- **von Klitzing, Klaus**
  Katzenbachstrasse 121; D-70563 Stuttgart; (DE)

Legal Representative:

- **Heusler, Wolfgang, Dipl.-Ing. (5441)**
  v. Bezold & Sozien Patentanwalte Akademiestrasse 7; 80799 Munchen; (DE)

	Country	Number	Kind	Date	

Patent	EP	704710	A1	19960403	(Basic)
	EP	704710	B1	20030205	
Application	EP	94115388		19940929	
Priorities	EP	94115388		19940929	

Designated States:
DE; FR; GB; IT; NL;

International Patent Class (V7): G01R-033/07**Abstract Word Count:** 134
NOTE: 6
NOTE: Figure number on first page: 6

Type	Pub. Date	Kind	Text

Publication: English
Procedural: English
Application: English

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB96	28
SPEC A	(English)	EPAB96	9701
CLAIMS B	(English)	200306	274
CLAIMS B	(German)	200306	283
CLAIMS B	(French)	200306	328
SPEC B	(English)	200306	9804
Total Word Count (Document A) 9731			
Total Word Count (Document B) 10689			
Total Word Count (All Documents) 20420			

Specification: ...quadruple injection device in separating the piezoresistive and Hall ("off-diagonal") voltages, while minimizing the **voltage** contact misalignment **offset**, in devices including a hole. (a) A rotationally **symmetric** device with a hole, e.g., annulus, and contacts within the interior boundary and outside...as dual current generators. Indeed, upon orienting the current directions as shown, one realizes a **Hall device** with minimal misalingment offset. In (c), we have generalized this idea to a biaxial quadruple...This is the essential equivalent circuit. (b) A special embodiment of the integrated photocurrent generator-**Hall device**. A buried n- type channel constitutes the electrically conductive material where the off-diagonal component...

Specification: ...quadruple injection device in separating the piezoresistive and Hall ("off-diagonal") voltages, while minimizing the **voltage** contact misalignment **offset**, in devices including a hole. (a) A rotationally **symmetric** device with a hole, e.g., annulus, and contacts within the interior boundary and outside...as dual current generators. Indeed, upon orienting the current directions as shown, one realizes a **Hall device** with minimal misalingment offset. In (c), we have generalized this idea to a biaxial quadruple... ...This is the essential equivalent circuit. (b) A special embodiment of the integrated photocurrent generator-**Hall device**. A buried n- type channel constitutes the electrically conductive material where theoff-diagonal component (Hall...

20/3K/3 (Item 3 from file: 348) **Links**
EUROPEAN PATENTS

00394069
Linearized differential amplifier
Linearisierter Differenzverstarker
Amplificateur differentiel linearise
Linearized differential **amplifier**

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	Country	Number	Kind	Date	
Patent	EP	400650	A2	19901205	(Basic)
	EP	400650	A3	19910502	
	EP	400650	B1	19961009	
Application	EP	90110372		19900531	
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	JP	89234615		19890912	

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International Patent Class (V7): H03F-003/45; H03F-001/32; **Abstract** ...A2

Abstract Word Count: 167

Type	Pub. Date	Kind	Text

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Procedural: English
Application: English

Available Text	Language	Update	Word Count
CLAIMS A	(English)		1260
SPEC A	(English)		13448
CLAIMS B	(English)	EPAB96	907
CLAIMS B	(German)	EPAB96	799
CLAIMS B	(French)	EPAB96	963
SPEC B	(English)	EPAB96	13171
Total Word Count (Document A) 14709			
Total Word Count (Document B) 15840			
Total Word Count (All Documents) 30549			

Specification: ...A3

LINEARIZED DIFFERENTIAL **AMPLIFIER**

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a **linearized** differential **amplifier** which can provide a constant transconductance in a wide range.

Description of the Prior Art...input range of 1 volt. As an example of composing a filter using such a **linearized** differential **amplifier**, there is "Multiple purpose filter" disclosed in Japanese Patent Application for Disclosure No. 58-161413... ...The method can provide an extremely wide linear range substantially equal to that of the **linearized** differential **amplifier** with the gain cell, and can guarantee a preferable S/N ratio.

The principle of... ...OF THE INVENTION

Therefore, it is an object of the present invention to provide a **linearized** differential **amplifier** which has a wide linear operation range and a high input impedance.

To achieve the object, a **linearized** differential **amplifier** according to the present invention is characterized by a differential amplifier composed in parallel connections... ...in the differential pair gives maximum value corresponding to an input voltage equals to the **offset voltag**.

The transconductance **value** is **symmetrical** with respect to the input **voltage** set at the **offset voltage**, and monotonously decreases in relation to the input voltage becomes larger or smaller than the...the differential amplifier according to the present invention is sufficiently practical.

As stated above, the **linearized** differential **amplifier** of the present invention has a wide linear operation range and can guarantee a high... ...Fig.1,

Fig.3 is a circuit diagram to show schematic entire composition of a **linearized** differential **amplifier** of the present invention,

Figs.4A, 4B and 4C are circuit diagrams to respectively show... ...to be used in the present invention,

Fig.5 is a circuit diagram of a **linearized** differential **amplifier** (comprising three differential pairs) which is a first embodiment of the present invention,

Fig.6 is a circuit diagram of a differential pair in the **linearized** differential **amplifier** of the first embodiment,

Figs.7A and 7B are diagrams to show relations of the Fig.6,

Fig.8 is a circuit diagram to show a modified example of the **linearized** differential **amplifier** shown in Fig.6,

Fig.9 is a circuit diagram of a **linearized** differential **amplifier** which is a second embodiment of the present invention,

Figs.10A and 10B are circuit diagrams to respectively show offset voltage generating means in the **linearized** differential **amplifier** of the present invention,

Fig.11 is a circuit diagram of a differential amplifier in... ...10B is used,

Fig.13A is a diagram to show comparison of transconductances in the **linearized** differential **amplifier** of the first embodiment in the present invention (using the equal ripple approximation and the maximally flat approximation) and the conventional **linearized** differential **amplifier**,

Fig.13B is a partly enlarged diagram of Fig.13A,

Fig.14 is a circuit... ...18B is used,

Fig.21A is a diagram to show comparison of transconductances in the **linearized** differential **amplifier** of the third embodiment in the present invention (using the equal ripple approximation and the maximally flat approximation) and the conventional **linearized** differential **amplifier**,

Fig.21B is a partly enlarged diagram of Fig.21A,

Fig.22 is a diagram... ...Fig.26 shows measurement results on the frequency characteristic of an active filter of the **linearized** differential **amplifier** as shown in Fig.25,

Fig.27 is a circuit diagram of the active filter ... ...diagram of an integrating circuit.

DETAILED DESCRIPTION OF THE EMBODIMENT

Hereinafter, an embodiment of a **linearized** differential **amplifier** of the present invention will be described.

The linearization in the **linearized** differential **amplifier** of the present invention basically comprises using a **linearized** differential **amplifier** schematically shown in Fig.3, preparing a plurality (N pairs) of the differential amplifiers so... ...the differential amplifier shown in Fig.2B, and adding them with weighting.

Namely, in the **linearized** differential **amplifier** shown in Fig.3, N pairs (where N is an integer of 3 or more...sup 4)(x) - 136tanh(sup 2)(x) + 16 (12)

Hereinafter, composition and operation of a **linearized** differential **amplifier** having three sets of differential pairs will be described as a first embodiment of the present invention.

Fig.5 is a schematical diagram of a **linearized** differential **amplifier** which is a first embodiment of the present invention, and Fig.6 is a circuit diagram of differential pairs in the **linearized** differential **amplifier** shown in Fig.5. In these diagrams, reference numeral 15 shows a load, 16A, 16B...the same drawing, it seen that the curve 28(min) of the transconductance of the **linearized** differential **amplifier** in the embodiment provides a wide linear operation range which is six times or more... ...be described with reference to Fig.9. Fig.9 is a circuit diagram of a **linearized** differential **amplifier** which is a second embodiment of the present invention. In the same drawing, emitter areas ... ...sub(T))log(sub(e))(M) (26)

Accordingly, these asymmetrical differential pairs become equivalent to **symmetrical** differential pairs apparently having an **offset voltage** of V(sub(T))log(sub(e))(M).

In the case of this embodiment, M... ...any given temperature.

As stated above, Fig.9 is a circuit diagram schematically showing a **linearized** differential **amplifier** as a second embodiment of the present invention. In the same diagram, the **linearized** differential **amplifier** is different from those in Fig.6 and Fig.8 in that the offset voltage...compared to the simple differential pair, and about 1.7 times as compared to the **linearized** differential **amplifier** using two sets of conventional differential pairs.

Heretofore, only the conditions to realize the maximally... ...by allowing the waving. Accordingly, an embodiment for realizing the equal ripple approximation in the **linearized** differential **amplifier** related to the present invention will be described hereinafter.

Analytical conditions concerning parameters necessary for ... ...to another load connected to the output terminal 4.

Next, composition and operation of the **linearized** differential **amplifier** as a third embodiment of the present invention using four sets of differential pairs will...simple differential pair or about 2.32 times as compared to the case of the **linearized** differential **amplifier** where conventional two sets of differential pairs are used.

As understood from the above description... ...approximation can be obtained. Therefore, an embodiment for realizing the equal ripple approximation on the **linearized** differential **amplifier** using four sets of differential pairs will be described next.

It is possible to introduce... ...input terminals 1, 2.

(2) Embodiment as a multiplier

The linear operation range of the **linearized** differential **amplifier** of the present invention is markedly wide as compared to the conventional differential pair, but... ...the Gilbert's gain cell requires a lowest operation voltage of at least 2V, the **linearized** differential **amplifier** according to this invention can be operated even at about 1V. Thus, it is possible ... ...present invention. In the same drawing, reference numerals 230, 231, and 232 respectively show the **linearized** differential **amplifier** according to this invention, for example, the one described in Fig.9. Moreover, it should... ...input signal source 233 generates a differential output current by the transconductance of the second **linearized** differential **amplifier** 230. Then, the differential output current is arranged by transistors 236, 237 provided by diode... ...linear operation range ten times or more at a relatively low voltage by using the **linearized** differential **amplifier** of the present invention.

In this embodiment, though the first and third differential amplifiers are... ...123 to obtain the same operation as shown in Fig.23. However, since the central **linearized** differential **amplifier** is composed of NPN transistors, it is necessary to change the transistor and the current... ...the differential amplifier having the conventional emitter degeneration resistor can be used in the central **linearized** differential **amplifier** 230 alone in the Figs.23 and 29.

(3) Embodiment as a filter

The **linearized** differential **amplifier** of the present invention can be also used as a variable transconductor. Accordingly, as shown...literature. In the same drawing, each of triangle symbols shows a transconductor, and specifically, the **linearized** differential **amplifier** of the present invention (in this case, N = 4) is used as the transconductor. In the same literature, since a conventional **linearized** differential **amplifier** in case of N = 2 is used, this embodiment can guarantee the linear operation range two times or more as wide as the conventional one. Actually, since the **linearized** differential **amplifier** has an offset voltage of about several millivolts to 10mV, the linear operation range becomes narrow so much. Namely, though the conventional **linearized** differential **amplifier** has a linear operation range of only about 30mV, the range of the **linearized** differential **amplifier** according to the present invention is about 100mV.

Fig.26 shows measurement results on the... ...active filter prepared based on the circuit of Fig.27 to which is applied a **linearized** differential **amplifier** of Fig.25 related to this invention. In the same diagram, the input voltage is.....by the weigting means are disclosed for fixed and variable cases.

The transconductance of the

linearized differential **amplifier** according to the invention is given by sum of transconductance of each of the differential pairs which form the entire **linearized** differential **amplifier**. Accordingly, the total transconductance is inversly proportional to absolute temperature T as it is clear... ...of absolute temperature T.

In the following embodiment, a method by which transconductance of the **linearized** differential **amplifier** according to the invention is not changed by a change of temperature will be explained... ...degree. It therefore is difficult to reduce the temperature coefficient of the transconductance of the **linearized** differential **amplifier**, using the resistor within the IC.

Accordingly, a resistor having smaller temperature coefficient may be...flat feature of the transconductance of the differential amplifier 320 can be obtained. In the **linearized** differential **amplifier** 320 as above described, the resistor 321 only having a smaller temperature coefficient is installed...

Specification: ...B1

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a **linearized** differential **amplifier** of the type as specified in the preamble of claim 1.

Decription of the Prior Art

A **linearized** differential **amplifier** of the aforementioned type is known from DE-A-3 027 071.

Generally, emitter coupled...input range of 1 volt. As an example of composing a filter using such a **linearized** differential **amplifier**, there is "Multiple purpose filter" disclosed in Japanese Patent Application for Disclosure No. 58-161413 ... ...The method can provide an extremely wide linear range substantially equal to that of the **linearized** differential **amplifier** with the gain cell, and can guarantee a preferable S/N ratio.

The principle of... ...SUMMARY OF THE INVENTION

It is an object of the present invention to provide a **linearized** differential **amplifier** of the type as described initially hereinabove in which **linearized** differential **amplifier** the offset magnitudes provided to each of the differential pairs and the ratio of the... ...specified optimum value.

This object is achieved by providing the features of claim 1.

The **linearized** differential **amplifier** according to this invention may have a wide linear operation range and a high input impedance.

In particular, a **linearized** differential **amplifier** according to the present invention may be realized by a differential amplifier composed in parallel... ...in the differential pair gives maximum value corresponding to an input voltage equals to the **offset voltage**.

The transconductance **value** is **symmetrical** with respect to the input **voltage** set at the **offset voltage**, and monotonously decreases in relation to the input voltage becomes larger or smaller than the...the differential amplifier according to the present invention is sufficiently practical.

As stated above, the **linearized** differential **amplifier** of the present invention has a wide linear operation range and can guarantee a high Fig.1,

Fig.3 is a circuit diagram to show schematic entire composition of a **linearized** differential **amplifier** of the present invention,

Figs.4A, 4B and 4C are circuit diagrams to respectively show... ...to be used in the present invention,

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Fig.8 is a circuit diagram to show a modified example of the **linearized** differential **amplifier** shown in Fig.6,

Fig.9 is a circuit diagram of a **linearized** differential **amplifier** which is a second embodiment of the present invention,

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Fig.13A is a diagram to show comparison of transconductances in the **linearized** differential **amplifier** of the first embodiment in the present invention (using the equal ripple approximation and the maximally flat approximation) and the conventional **linearized** differential **amplifier**,

Fig.13B is a partly enlarged diagram of Fig.13A,

Fig.14 is a circuit... ...18B is used,

Fig.21A is a diagram to show comparison of transconductances in the **linearized** differential **amplifier** of the third embodiment in the present invention (using the equal ripple approximation and the maximally flat approximation) and the conventional **linearized** differential **amplifier**,

Fig.21B is a partly enlarged diagram of Fig.21A,

Fig.22 is a diagram... ...by simulation of a input-output characteristics,

Fig.25 is a circuit diagram of an **linearized** differential **amplifier** (N=4) according to the invention,

Fig.26 shows measurement results on the frequency characteristic of an active filter of the **linearized** differential **amplifier** as shown in Fig.25,

Fig.27 is a circuit diagram of the active filter... ...diagram of an integrating circuit.

DETAILED DESCRIPTION OF THE EMBODIMENT

Hereinafter, an embodiment of a **linearized** differential **amplifier** of the present invention will be described.

The linearization in the **linearized** differential **amplifier** of the present invention basically comprises using a **linearized** differential **amplifier** schematically shown in Fig.3, preparing a plurality (N pairs) of the differential amplifiers so... ...the differential amplifier shown in Fig.2B, and adding them with weighting.

Namely, in the **linearized** differential **amplifier** shown in Fig.3, N pairs (where N is an integer of 3 or more...omitted) (Formula omitted) (Formula omitted) (Formula omitted) (Formula omitted)

Hereinafter, composition and operation of a **linearized** differential **amplifier** having three sets of differential pairs will be described as a first embodiment of the present invention.

Fig.5 is a schematical diagram of a **linearized** differential **amplifier** which is a first embodiment of the present invention, and Fig.6 is a circuit diagram of differential pairs in the **linearized** differential **amplifier** shown in Fig.5. In these diagrams, reference numeral 15 shows a load, 16A, 16B...the same drawing, it seen that the curve 28(minutes) of the transconductance of the **linearized** differential **amplifier** in the embodiment provides a wide linear operation range which is six times or more... ...be described with reference to Fig.9. Fig.9 is a circuit diagram of a **linearized** differential **amplifier** which is a second embodiment of the present invention. In the same drawing, emitter areas... ...be)) is expressed as follows. (Formula omitted)

Accordingly, these asymmetrical differential pairs become equivalent to **symmetrical** differential pairs apparently having an **offset voltage** of V(sub(T))log(sub(e))(M).

In the case of this embodiment, M... ...any given temperature.

As stated above, Fig.9 is a circuit diagram schematically showing a **linearized** differential **amplifier** as a second embodiment of the present invention. In the same diagram, the **linearized** differential **amplifier** is different from those in Fig.6 and Fig.8 in that the offset voltage...compared to the simple differential pair, and about 1.7 times as compared to the **linearized** differential **amplifier** using two sets of conventional differential pairs.

Heretofore, only the ...by allowing the waving. Accordingly, an embodiment for realizing the equal ripple approximation in the **linearized** differential **amplifier** related to the present invention will be described hereinafter.

Analytical conditions concerning parameters necessary for... ...to another load connected to the output terminal 4.

Next, composition and operation of the **linearized** differential **amplifier** as a third embodiment of the present invention using four sets of differential pairs will...simple differential pair or about 2.32 times as compared to the case of the **linearized** differential **amplifier** where conventional two sets of differential pairs are used.

As understood from the above description ... ...approximation can be obtained. Therefore, an embodiment for realizing the equal ripple approximation on the **linearized** differential **amplifier** using four sets of differential pairs will be described next.

It is possible to introduce...input terminals 1, 2.

(2) Embodiment as a multiplier

The linear operation range of the **linearized** differential **amplifier** of the present invention is markedly wide as compared to the conventional differential pair, but... ...the Gilbert's gain cell requires a lowest operation voltage of at least 2V, the **linearized** differential **amplifier** according to this invention can be operated even at about 1V. Thus, it is possible... ...present invention. In the same drawing, reference numerals 230, 231, and 232 respectively show the **linearized** differential **amplifier** according to this invention, for example, the one described in Fig.9. Moreover, it should... ...input signal source 233 generates a differential output current by the transconductance of the second **linearized** differential **amplifier** 230. Then, the differential output current is arranged by transistors 236, 237 provided by diode...linear operation range ten times or more at a relatively low voltage by using the **linearized** differential **amplifier** of the present invention.

In this embodiment, though the first and third differential amplifiers are... ...123 to obtain the same operation as shown in Fig.23. However, since the central **linearized** differential **amplifier** is composed of NPN transistors, it is necessary to change the transistor and the current... ...the differential amplifier having the conventional emitter degeneration resistor can be used in the central **linearized** differential **amplifier** 230 alone in the Figs.23 and 29.

(3) Embodiment as a filter

The **linearized** differential **amplifier**

of the present invention can be also used as a variable transconductor. Accordingly, as shown... ...literature. In the same drawing, each of triangle symbols shows a transconductor, and specifically, the **linearized** differential **amplifier** of the present invention (in this case, N = 4) is used as the transconductor. In the same literature, since a conventional **linearized** differential **amplifier** in case of N = 2 is used, this embodiment can guarantee the linear operation range two times or more as wide as the conventional one. Actually, since the **linearized** differential **amplifier** has an offset voltage of about several millivolts to 10mV, the linear operation range becomes narrow so much. Namely, though the conventional **linearized** differential **amplifier** has a linear operation range of only about 30mV, the range of the **linearized** differential **amplifier** according to the present invention is about 100mV.

Fig.26 shows measurement results on the... ...active filter prepared based on the circuit of Fig.27 to which is applied a **linearized** differential **amplifier** of Fig.25 related to this invention. In the same diagram, the input voltage is ... ...by the weigting means are disclosed for fixed and variable cases.

The transconductance of the **linearized** differential **amplifier** according to the invention is given by sum of transconductance of each of the differential pairs which form the entire **linearized** differential **amplifier**. Accordingly, the total transconductance is inversly proportional to absolute temperature T as it is clear... ...of absolute temperature T.

In the following embodiment, a method by which transconductance of the **linearized** differential **amplifier** according to the invention is not changed by a change of temperature will be explained...degree. It therefore is difficult to reduce the temperature coefficient of the transconductance of the **linearized** differential **amplifier** using the resistor within the IC.

Accordingly, a resistor having smaller temperature coefficient may be...32 shows a specific compositional diagram of an amplifier circuit as an application of the **linearized** differential **amplifier** according to the invention.

This circuit comprises a combination of the current generating means 300B ... ...flat feature of the transconductance of the differential amplifier 320 can be obtained. In the **linearized** differential **amplifier** 320 as above described, the resistor 321 only having a smaller temperature coefficient is installed...

Claims: ...A3

1. A **linearized** differential **amplifier**, comprising:

arranging N (N is an integer of 3 or more) sets of differential pairs... ...of differential pairs(16) respectively; and

means(19) for adding the output currents.

2. A **linearized** differential **amplifier** according to claim 1, wherein

the means(17) for supplying offset voltages and the means... ...the differential output current corresponding to change of the differential input voltage inputted to the **linearized amplifier** shows a flat characteristic.

3. A **linearized** differential **amplifier** according to claim 1, wherein

the means(17) for supplying offset voltages and the means... ...the differential output current corresponding to change of the differential input voltage inputted to the **linearized amplifier** shows an equal ripple characteristic.

4. A **linearized** differential **amplifier** according to claim 2, wherein

the currents to be weighted by the weighting means(18... ...to respective emitters commonly connected in the N sets of differential pairs(16).

5. A **linearized** differential **amplifier** according to claim 3, wherein

the currents to be weighted by the weighting means(18... ...to respective emitters commonly connected in the N sets of differential pairs(16).

6. A **linearized** differential **amplifier** according to claim 4, wherein

the number of the N sets of differential pairs is... ...1016A, 1016B, 1016C, and 1016D) is about 1 : 0.5478 : 0.5478 : 1.

7. A **linearized** differential **amplifier** according to claim 1, wherein

the means(17) for supplying different and equivalent offset voltages is operated by changing emitter areas of transistors which are compositional elements of the **linearized** differential **amplifier**.

8. A **linearized** differential **amplifier** according to claim 7, wherein

the number of diffrential pairs of the N sets is... ...1:13.40261, 1:2.030215, 2.030215, and 13.40261:1, respectivery.

9. A **linearized** differential **amplifier** according to claim 1, wherein

the means(19) for adding the output currents of the... ...which the output terminals of the differential pairs are connected to each other.

10. A **linearized** differential **amplifier** according to claim 1, wherein

the means(18) for weighting the output currents is operated... ...obtained by changing proportionally the operational current of all of the differential pairs.

11. A **linearized** differential **amplifier** according to claim 1, wherein the bipolar transistors are composed of silicon transistor.

12. A **linearized** differential **amplifier** according to claim 1, wherein the bipolar transistors are composed of silicon heterobipolar transistor.

13. A **linearized** differential **amplifier** according to claim 1, wherein the bipolar transistors are composed of Gallium-Arsenide-heterobipolar transistor.

14. A **linearized** differential **amplifier** according to claim 1, wherein the means for weighting is operated by changing in propotional to the absolute temperature the operational current of all of the differential pairs.

15. A **linearized** differential **amplifier**, comprising:

arranging three sets of differential pairs (16A, 16B, and 16C) respectively composed of bipolar... ...16A, 16B, and 16C), respectively; and

means(19) for adding the output currents.

16. A **linearized** differential **amplifier** according to claim 15, wherein

the means(17) for supplying offset voltages and the means... ...the differential output current corresponding to change of the differential input voltage inputted to the **linearized amplifier** shows a flat characteristic.

17. A **linearized** differential **amplifier** according to claim 16, wherein

the means(17) for supplying offset voltages and the means... ...the differential output current corresponding to change of the differential input voltage inputted to the **linearized** differential **amplifier** shows a equal ripple characteristic.

18. A **linearized** differential **amplifier** according to claim 16, wherein

the currents to be weighted by the weighting means(18...commonly connected in the three sets of differential pairs (16A, 16B, and 16C).

19. A **linearized** differential **amplifier** according to claim 17, wherein

the currents to be weighted by the weighting means(18... ...commonly connected in the three sets of differential pairs (16A, 16B, and 16C).

20. A **linearized** differential **amplifier** according to claim 18, wherein

the equivalent offset voltages to be given to the three... ...and 16C) to the second differential pair(16B) is about 0.64 times.

21. A **linearized** differential **amplifier** according to claim 15, wherein

the means(17) for supplying different and equivalent offset voltages is operated by changeing emitter areas of transistors which are compositional elements of the **linearized** differential **amplifier**.

22. A **linearized** differential **amplifier** according to claim 21, wherein

ratio of the emitter areas of the transistors which make... ...sets is 1:7.872983, and 1:1, and 7.872983:1, respectively.

23. A **linearized** differential **amplifier** according to claim 15, wherein

the means(19) for adding the output currents of the... ...of the differential pairs(16A, 16B, and 16C) are connected to each other.

24. A **linearized** differential **amplifier** according to claim 15, wherein

the means(17) for weighting the output currents is operated... ...the operational current of all of the differential pairs(16A, 16B, and 16C).

25. A **linearized** differential **amplifier** according to claim 15, wherein the bipolar transistors are composed of silicon transistor.

26. A **linearized** differential **amplifier** according to claim 15, wherein the bipolar transistors are composed of silicon-heterobipolar transistor.

27. A **linearized** differential **amplifier** according to claim 15, wherein the bipolar transistors are composed of Gallium-Arsenide-heterobipolar transistor.

28. A **linearized** differential **amplifier** according to claim 15, wherein the means for weighting is operated by changing in propotional...

Claims: ...B1

1. A **linearized** differential **amplifier**, comprising

differential pairs (16; 1016) of a number N of sets arranged in parallel and... ...coefficient until the highest order of the transconductance (see image in original document) of the **linearized** differential **amplifier** at x = 0 is set to zero or to approximately zero,

where x = -Vd/2V... ...pairs.)

(N/2) is a symbol expressing an integer part of N/2.

2. The **linearized** differential **amplifier** according to claim 1, characterized in that the supply means (17; 107) for supplying offest... ...differential pair (16; 1016) corresponding to a change of an input voltage input to the **linearized amplifier**, exhibits a flat characteristic.

3. The **linearized** differential **amplifier** according to claim 1, characterized in that the supply means (17; 107) for supplying offest... ...differential pair (16; 1016) corresponding to a change of an input voltage input to the **linearized amplifier**, exhibits an equal ripple characteristic.

4. The **linearized** differential **amplifier** according to claim 2 or 3, characterized in that the output currents to be weighted... ...respective emitters commonly connected to the N sets of differential pairs (16; 1016).

5. The **linearized** differential **amplifier** according to claim 2 or 3, characterized in that

the number of sets is N... ...fourth differential pairs (16; 1016) is about

1 : 0.5478 : 0.5478 : 1.

6. The **linearized** differential **amplifier** according to claim 1, characterized in that the supply means (17; 107) supplying different and... ...areas of transistors which are composition elements of each differential pair (16; 1016).

7. The **linearized** differential **amplifier** according to claim 6, characterized in that

the number of sets is N = 4; and... ...13.40261,

1 : 2.030215,

2.030215 : 1, and

13.40261 : 1, respectively.

8. The **linearized** differential **amplifier** according to claim 1, characterized in that the adding means (19; 109 for adding the... ...output terminals of the differential pairs (16; 1016) are connected to each other.

9. The **linearized** differential **amplifier** according to claim 1, characterized in that the weighting means (18; 108) is effected by... ...obtained by changing proportionally the operational currents of all of the differential pairs.

10. The **linearized** differential **amplifier** according to claim 1, characterized in that the bipolar transistors (5, 6; 105, 106) are composed of silicon transistors.

11. The **linearized** differential **amplifier** according to claim 1, characterized in that the bipolar transistors (5, 6; 105, 106) are composed of silicon heterobipolar transistors.

12. The **linearized** differential **amplifier** according to claim 1, characterized in that the bipolar transistors (5, 6; 105, 106) are composed of Gallium-Arsenid heterobipolar transistors.

13. The **linearized** differential **amplifier** according to claim 1, characterized in that the weighting means (18; 108) is effected by... ...currents of the differential pairs (16; 1016) in proportion to the absolute temperature.

14. The **linearized** differential **amplifier** according to Claim 6,

characterized in that

the number of sets is N =

20/3K/4 (Item 4 from file: 348) **Links**
EUROPEAN PATENTS

00366100
Symmetric integrated amplifier with controlled DC offset voltage.
Symmetrischer integrierter Verstarker mit gesteuerter Offset-Gleichspannung.
Amplificateur integre symetriquement a commande de tension continue de decalage.
Symmetric integrated **amplifier** with controlled DC **offset voltage**.

Patent Assignee:

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Inventor:

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Legal Representative:

- **Buckley, Christopher Simon Thirsk et al (28912)**
  AT&T (UK) LTD. AT&T Intellectual Property Division 5 Mornington Road; Woodford Green, Essex IG8 OTU; (GB)

	Country	Number	Kind	Date	
Patent	EP	348079	A2	19891227	(Basic)
	EP	348079	A3	19900822	
	EP	348079	B1	19930519	
Application	EP	89305852		19890609	
Priorities	US	209462		19880620	

Designated States:
DE; ES; FR; GB; NL; SE;

International Patent Class (V7): H03F-001/30; ; **Abstract** ...may all be formed with FET structures to minimize fabrication problems. In accordance with the **symmetric** arrangement of the present invention, the output DC **offset voltage** will be maintained at zero volts, regardless of the variations noted above. A multistage **symmetric amplifier** may then be formed simply by directly connecting a number of single stage symmetric amplifiers...

Abstract Word Count: 187

Type	Pub. Date	Kind	Text

Publication: English
Procedural: English
Application: English

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	632
CLAIMS B	(German)	EPBBF1	511
CLAIMS B	(French)	EPBBF1	720
SPEC B	(English)	EPBBF1	3159
Total Word Count (Document A) 0			
Total Word Count (Document B) 5022			
Total Word Count (All Documents) 5022			

Specification: ...B1

Background of the Invention

1. Field **of the** Invention

The present invention relates to a **symmetric** integrated **amplifier** with controlled DC **offset voltage and**, more **particularly**, to such an **amplifier which** is insensitive to variations in either the power supply voltages or transistor threshold voltage.

2... remaining in the prior art is addressed by the present invention which relates to a **symmetric** integrated **amplifier** with controlled **voltage offset and**, more **particularly**, to such **an amplifier** which is insensitive to variations in either the power supply voltages or transistor threshold voltages.

In accordance with the present invention, a **symmetric amplifier** arrangement is disclosed which provides (**in the** quiescent state) an identical voltage drop between each power supply (VDD,VSS) and the amplifier... ...voltage of conventional JFET amplifiers formed in InP may also vary. This variation in DC **offset** voltage makes the formation of any **type of** multi-stage amplifier impossible. An advantage of the **symmetric arrangement** of the present invention is **that** virtually no DC **offset voltage** is present if the portion of the circuit connected between VDD and the output is... ...this same output node. Thus, a multi-stage amplifier may be formed when utilizing the **symmetric** arrangement of the present invention merely by directly coupling single stage amplifiers together in series ... ...invention;

FIG. 2 is a graph illustrating the amplifier transfer curve and gain of the **inventive symmetric amplifier** arrangement of FIG. 1;

FIG. **3 is** a graph of DC **offset voltage** as a function of JFET threshold voltage for both a prior art arrangement and the inventive symmetric arrangement of FIG. 1; and

FIG. 4 illustrates an exemplary multistage **symmetric amplifier** formed in accordance with the **present invention**. acceptable.

Detailed Description

A **symmetric amplifier** configuration of the present invention **is as** illustrated in FIG. 1. **Symmetric amplifier** 30, like the Hornbuckle et **al. amplifier** discussed above, utilizes a common source FET to provide the amplifier gain. In particular, an...the problems associated with the prior art are eliminated by forming amplifier 30 as a **symmetrical amplifier**. In particular, the input branch **of the amplifier** including input FET 32 and active load FET 34 is balanced by a pair of... ...of changes in the power supply voltage from 5V through 9V. Note that for the **symmetric amplifier** arrangement of the present invention, **the various** transfer curves cross at V(sub(IN))=V(sub(OUT))=0V, instead of merging at the extreme negative DC **offset** voltage level, as is typical for **prior art** amplifiers.

Another advantage of the **symmetrical** arrangement of the present invention, as discussed above, is that it is insensitive to variations... ...given VSS=VDD). This graph is a result of computer simulations of a prior art **amplifier** and **symmetrical amplifier** 30 of FIG. **1**, utilizing **the values** associated with typical InP-based FETs. As seen by reference to FIG. 3, the DC... ...to a value of +0.18V for a threshold voltage V(sub(th)) of approximately **-1.0V**. In contrast, the DC **offset voltage** of **symmetric** amplifier 30 remains **at** 0V, regardless **of threshold voltage value**.

As discussed above, an **advantage of the** amplifier configuration of the present invention is that a zero DC **offset** voltage is obtained by virtue of its **symmetrical** circuit arrangement. Therefore, a **symmetric** amplifier **may** be fabricated which exhibits **a** 0V DC offset, regardless of changes in supply **voltage or** transistor **threshold voltage**. With this **ability** to reproducibly **provide a** 0V DC **offset**, a multistage **symmetric** amplifier may be **formed** simply by **connecting a** number of single stage amplifiers together in series. One such multistage **symmetric amplifier** is illustrated in FIG. 4.

Referring to FIG. 4, a multistage **symmetric amplifier** 50 is shown which includes **a first** (or input) stage 52, a second stage 54, and a third (or output) stage 56... of the gain provided by each stage.

It is to be understood that although the **symmetrical amplifier** design of the present invention **was described** as particularly advantageous when fabricated with InP-based FETs, various other materials, including but not limited to GaAs, may be utilized to form the **symmetric amplifier** arrangement of the present invention **and enjoy** the same benefits of threshold voltage and supply voltage insensitivity.

20/3K/5 (Item 5 from file: 348) Links
EUROPEAN PATENTS

00357504
Integrated low-pass filter arrangement.
Integrierte Tiefpass-Filterschaltung.
Circuit de filtrage passe-bas integre.
Integrated low-pass **filter** arrangement.

Patent Assignee:

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Legal Representative:

- **Peters, Rudolf Johannes et al (49051)**
  INTERNATIONAAL OCTROOIBUREAU B.V., Prof. Holstlaan 6; NL-5656 AA Eindhoven; (NL)

	Country	Number	Kind	Date	
Patent	EP	329245	A1	19890823	(Basic)
	EP	329245	B1	19950510	
Application	EP	89200342		19890213	
Priorities	NL	88421		19880219	

Designated States:
DE; FR; GB; IT; NL;

International Patent Class (V7): H03H-007/06; H03H-011/46; **Abstract** ...A1

Abstract Word Count: 104

Type	Pub. Date	Kind	Text

Publication: English
Procedural: English
Application: Dutch

Available Text	Language	Update	Word Count
CLAIMS A	(English)		317
SPEC A	(English)		3826
CLAIMS B	(English)	EPAB95	353
CLAIMS B	(German)	EPAB95	287
CLAIMS B	(French)	EPAB95	391
SPEC B	(English)	EPAB95	3998
Total Word Count (Document A) 4143			
Total Word Count (Document B) 5029			
Total Word Count (All Documents) 9172			

Specification: ...A1

Integrated low-pass **filter** arrangement.

The invention relates to an **integrated filter** arrangement comprising a resistor section between the input and the output of the arrangement and... ...example, with reference to the accompanying Figures.

Fig. 1 shows a basic diagram of the **integrated** low-pass **filter** in accordance with the invention.

Fig. 2 shows a voltage-current characteristic of an anti...resistance is utilised in order to attain a very low cut-off frequency.

If the **filter** is **integrated** this will inevitably lead to a leakage current leakage current will inevitably occur from the... ...between the input voltage and the output voltage of the filter. The use of a **symmetrical** filter arrangement enables said **offset voltage** to be reduced substantially, or even to be eliminated completely.

Fig. 3 shows an example...

Specification: ...B1

The invention relates to an **integrated** low-pass **filter** arrangement comprising an input terminal, an output terminal, a resistor section connected between the input... ...offset between the input voltage and the output voltage, it is preferred to utilise an **integrated** low-pass **filter** arrangement, comprising a first input terminal, a second input terminal a first output terminal, a...example, with reference to the accompanying Figures.

Fig. 1 shows a basic diagram of the **integrated** low-pass **filter** in accordance with the invention.

Fig. 2 shows a voltage-current characteristic of an anti... ...resistance is utilised in order to attain a very low cut-off frequency.

If the **filter** is **integrated** this will inevitably lead to a leakage current leakage current will inevitably occur from the... ...between the input voltage and the output voltage of the filter. The use of a **symmetrical** filter arrangement enables said **offset voltage** to be reduced substantially, or even to be eliminated completely.

Fig. 3 shows an example...

Claims: ...A1

1. An **integrated** low-pass **filter** arrangement comprising a resistor section between the input and the output of the arrangement and... ...characterized in that the resistor section comprises two diodes arranged in anti-parallel.

2. An **integrated** low-pass **filter** arrangement comprising two resistor sections each connected between an input terminal of the input and... ...that each of the resistor sections comprises two diodes arranged in anti-parallel.

3. An **integrated** low-pass **filter** circuit as claimed in Claim 1 or 2, characterized in that each anti-parallel array... ...input terminal, and each having its emitter connected to the respective output terminal.

4. An **integrated** low-pass **filter** arrangement comprising a resistor section between the input and the output of the arrangement and... ...poled in the forward direction for the leakage current through the resistor section.

5. An **integrated** low-pass **filter** arrangement, comprising two resistor sections each arranged between an input terminal of the arrangement and... ...in the forward direction for the leakage current through the relevant resistor section.

6. An **integrated** low-pass **filter** arrangement as claimed in Claim 4 or 5, characterized in that the diode(s) in... ...s) is (are) constituted by transistor whose base-collector junction is short-circuited.

7. An **integrated** low-pass **filter** arrangement as claimed in any one of the preceding Claims, characterized in that the capacitor...

Claims: ...B1

1. An **integrated** low-pass **filter** arrangement comprising an input terminal (k1), an output terminal (k2), a resistor section connected between... ...section and is operating around the zero point of its voltage-current characteristic.

2. An **integrated** low-pass **filter** arrangement, comprising a first input terminal (k4), a second input terminal (k5) a first output... ...and which is operating around the zero point of its voltage-current characteristic.

3. An **integrated** low-pas **filter** arrangement as claimed in claim 1 or 2, characterized in that the resistor section comprises... ...parallel and also operating around the zero point of its voltage-current characteristic.

4. An **integrated** low-pass **filter** arrangement as claimed in Claim 3, characterized in that each anti-parallel array of diodes... ...and each having its emitter connected to the respective output terminal (k6, k7).

5. An **integrated** low-pass **filter** arrangement as claimed in Claim 1 or 2, characterized in that the diode(s) in... ...constituted by a transistor (T2; T4) whose base-collector junction is short-circuited.

6. An **integrated** low-pass **filter** arrangement as claimed in any one of the preceding Claims, characterized in that the capacitor...

20/3K/6 (Item 6 from file: 348) Links
EUROPEAN PATENTS

00275339
Improved structure for Hall device.
Struktur fur Hallanordnung.
Structure pour un dispositif a effet Hall.
Improved structure for **Hall device**.

Patent Assignee:

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Legal Representative:

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  Schlumberger Industries Centre de Recherche/SMR B.P. 620-05; F-92542 Montrouge Cedex; (FR)

	Country	Number	Kind	Date	
Patent	EP	269510	A2	19880601	(Basic)
	EP	269510	A3	19890524	
Application	EP	87402585		19871117	
Priorities	US	933444		19861121	

Designated States:
AT; BE; CH; DE; ES; FR; GB; GR; IT; LI;
LU; NL; SE;

International Patent Class (V7): H01L-043/06; ; **Abstract** ...A2

Abstract Word Count: 124

Type	Pub. Date	Kind	Text

Publication: English
Procedural: English
Application: English

Available Text	Language	Update	Word Count
CLAIMS A	(English)		465
SPEC A	(English)		4355
Total Word Count (Document A) 4820			
Total Word Count (Document B) 0			
Total Word Count (All Documents) 4820			

Specification: ...A3

IMPROVED STRUCTURE FOR **HALL DEVICE**

Technical Field

The invention concerns Hall devices and, more particularly, an improved structure for a **Hall device** whereby first and second order voltage offsets can be eliminated or readily compensated.

Background Art... ...variously called the output, sensor or Hall voltage electrodes.

As is well known, when a **Hall device** is inserted into a magnetic field having a component normal to the plane of the... ...to a home or office. This is done by applying a excitation voltage to the **Hall device** which is proportional to the AG line voltage and by coupling one or more of... ...Hall effect device so that the strength of the magnetic field being applied to the **Hall device** is proportional to the current flowing in the measured live lines. The voltage appearing at... ...devices is a condition in which an output appears at the output electrodes of the **Hall device** even though no external magnetic field is present. Ideally, if no magnetic field were present and the **Hall device** were perfectly symmetrical, the output of a **Hall device** at its output electrodes would be zero, even when an excitation voltage is applied to... ...offset is a first order (linear) offset due to inhomogeneities in the material comprising the **Hall device**. This offset term can be readily compensated for by the use of external balancing resistors connected to the output electrodes of the **Hall device**. However, the other component of the voltage offset is a second order and non-linear function which is believed to be caused by alignment errors in the fabrication of the **Hall device**. Such alignment errors cause the **Hall device** to be formed having a somewhat asymmetrical shape. Other causes of this second order offset... ...of the Invention

In accordance with one aspect of the invention a structure for a **Hall device** comprises:

a main body formed from a material exhibiting the Hall effect;

at least a...error which might occur in the placement of the output electrodes during fabrication of the **Hall device**. This is done to ensure that at least two of the output electrodes will not... ...offset term by deliberately introducing asymmetry to the geometry of the electrode structure of the **Hall device**.

Although one of the electrodes can be disposed along the centerline, it is also possible... ...in conjunction with the accompanying drawings wherein:

Figure 1 shows a first embodiment of a **Hall device** constructed in accordance with the principles of the present invention;

Figure 2 shows a second... ...present invention having four output electrodes;and

Figure 4 shows an alternative embodiment of the **Hall device** shown in Figure 1.

Best Modes for Carrying Out the Invention

Ideally, a **Hall device** should have an output which is linear with respect to the input current, i, and... ...H)) is the Hall constant, d is the thickness of the plate making up the **Hall device**, and t is time.

In the case of a rectangular **Hall device**, equation 1 holds only if the length-to-width ratio of the sides of the...voltage are known, including the use of external potentiometers to balance the output of the **Hall device**, the use of multiple electrodes and trimming of the Hall electrodes to reduce X(sub... ...V.

In the past, attempts have been made to reduce or eliminate this first order **offset voltage** by making the **Hall device** more **symmetrical** and reducing electrode alignment errors. In another approach, some prior art devices have attempted to ... ...to overcome this first order or linear voltage offset in Hall devices, in a real **Hall device** (rho)(x) is not constant. This is especially true in the case of thin-film... ...compensated for by the use of external balancing resistors applied to the outputs of the **Hall device**. However, the K(sub 2)i(sup 2) term is non-linear and cannot be... ...in this fashion.

Turning now to Figure 1, there is shown a geometry for a **Hall device** constructed in accordance with the principles of the present invention which eliminates this nonlinear second... ...2)).

Surprisingly, the elimination of this second order term comes about by deliberately fabricating the **Hall device** with a carefully designed asymmetrical shape.

Hall device 1 comprises a generally rectangular body 3 of material exhibiting the Hall effect. Such materials... ...thin film of gallium arsenide, formed as shown in U.S. Patent 4,398,342.

Hall device 1 includes a pair of excitation electrodes 5 and 7 which are connected to a source of electrical voltage and current (not shown) for powering **Hall device** 1.

Hall device 1 further includes a first pair of output electrodes 9 and 11 disposed on one...trimming resistor 19 to eliminate the second order voltage offset term.

More particularly, for a **Hall device** at a given temperature, T, and an applied excitation voltage V, the conductivity of the... ...x, T and V. v(x) is the voltage at a position x along the **Hall device**. The valve of V where the Hall output voltage is taken is v(sub(H... ...in original document)

The V and V(sup 2) terms are of primary interest in **Hall device** applications. Therefore v(sub 2)(x) is defined as follows: (see image in original document)

For a standard **Hall device** having a rectangular body and point-contact type output electrodes the offset voltage V(sub...Figure 2 requires it be greater than (DELTA)X which would make an extremely long **Hall device** necessary in order to preserve the linearity of the device with respect to the magnetic... ...see image in original document) which has the same value range as a two electrode **Hall device**.

In the cases of both the three and four electrode devices (Figures 1-3) the... ...20, drawn between each electrode pair, is intentionally offset from the centerline 17 of the **Hall device** by a value whose magnitude is greater than or equal to the largest error which... ...to be point-type electrodes placed along the edges of rectangular body 3 of the **Hall device**. Where other **Hall device** shapes or Hall output electrodes of more substantial area are involved the analysis is somewhat... ...will still occur if the principles set forth above are followed.

Figure 4 shows a **Hall device** similar to that shown in Figure 1 which is a good approximation to the ideal... ...to body 3 and integral with the body. Also, it is not necessary that the **Hall device** have a rectangular shape. For example, rather than a rectangular shape, a rhombic or parallelpiped... ...and output electrodes. Thus, the principles of the present invention can be applied to other **Hall device** geometries.

Claims: ...A3

1. A structure for a **Hall device** characterized by:

a main body formed from a material exhibiting the Hall effect;

at least... ...between the excitation electrodes and through the electrical midpoint of the main body.

2. The **Hall device** according to claim 1, characterized in that at least two of the output electrodes are... ...largest expected error which might occur in the placement of the output electrodes.

3. The **Hall device** according to claim 1, characterized in that each of the output electrodes is offset from said centerline.

4. The **Hall device** according to claim 1, characterized in that there are two pairs of output electrodes, a... ...along the side of the body opposite the first pair of output electrodes.

5. The **Hall device** according to claim 4, characterized in that a line drawn equidistant between the first pair ... ...respect to a line drawn equidistant between the second pair of output electrodes.

6. The **Hall device** according to claim 4, characterized in that the first pair of output electrodes is disposed directly opposite the second pair of output electrodes.

7. The **Hall device** according to claim 5 or 6, characterized in that one output electrode of each of the pairs is centered along the centerline.

8. The **Hall device** according to any one of the preceding claims, characterized in that at least one balancing resistor is electrically connected between the first pair of output electrodes.

9. The **Hall device** according to any one of the preceding claims, characterized in that the main body has... ...of the main body coincides with the geometrical center of the main body.

10. The **Hall device** according to claim 9, characterized in that each of the output electrodes comprises a generally...

20/3K/7 (Item 7 from file: 348) Links
EUROPEAN PATENTS

00237235
Symmetrical bridge circuit for measuring mass air flow.
Symmetrische Bruckenschaltung zum Messen des Massendurchflusses von Luft.
Couplage en pont symetrique pour mesurer le debit massique d'air.

Patent Assignee:

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	Country	Number	Kind	Date	
Patent	EP	234298	A1	19870902	(Basic)
	EP	234298	B1	19920415	
Application	EP	87101015		19870124	
Priorities	US	830317		19860218	

Designated States:
DE; FR; GB; IT; SE;

International Patent Class (V7): G01F-001/68; G01P-005/12; **Abstract Word Count:** 273

Type	Pub. Date	Kind	Text

Publication: English
Procedural: English
Application: English

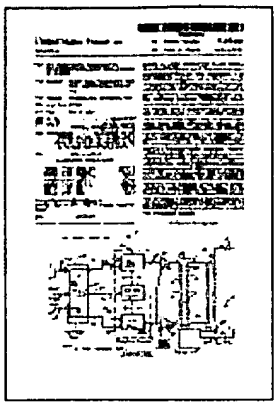
Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	519
CLAIMS B	(German)	EPBBF1	439
CLAIMS B	(French)	EPBBF1	637
SPEC B	(English)	EPBBF1	1485
Total Word Count (Document A) 0			
Total Word Count (Document B) 3080			
Total Word Count (All Documents) 3080			

Claims: ...including means (R23) electrically connected to one input of said control amplifier (ICIB) for causing **the** control **amplifier** to turn on said power driver (Q1) when the power supply to the circuit is

All monolithic transceiver operative from a low voltage VCC DC supply

Marc T. Stein et al

Patent summary



Read this patent

View patent at USPTO

Abstract | Drawing | Description | Claims

Abstract

A new and improved all monolithic transceiver manufactured on a single semiconductor die and operative from a 5 volt DC power supply. The transceiver meets all of the pulse width and timing requirements of the MIL-STD-1553 transceiver and is operative at high switching speeds and high output current levels to generate bi-phase TX OUT and TX OUT signals used to drive, respectively, two center tapped primary windings of an output transformer. The transmitter includes two dynamically driven data channels which are driven out of phase and in a controlled manner that ensures that one data channel has been completely turned off before the other data channel turns on, thereby maximizing power transfer and operating efficiency while minimizing unnecessary current drain and eliminating current spiking in the output of the transmitter. The receiver of the transceiver includes a differential amplifier connected to drive first a balanced differential filter and then a differential window...

Patent number: 5153466
Filing date: Mar 26, 1991
Issue date: Oct 6, 1992
Inventors: Marc T. Stein, Lonny E. Stormo

Claims

What is claimed is:

1. An integrated transmitter-receiver (transceiver) adapted for complete construction on a single semiconductor die and operative from a single 5 volt or equivalent DC supply voltage for providing a digital communication link between two or more computers, comprising:

a. a transmitter section having a low power transmission timer with a logic input stage therein for receiving bi-phase input digital data TX IN and TX IN,
b. first and second wave shaping stages connected to separate outputs of said logic input stage for controlling and being controlled by the rise and fall times of the output logic signals from said logic input stage and operative so that said first and second wave shaping stages conduct at mutually exclusive times, and
c. first and second output current drivers connected, respectively, to the outputs of said first and second wave shaping stages and operative for connection to the primary winding of a transformer which is center tapped to ground potential, whereby each one-half of said primary winding of said transformer is completely turned off by one of said current drivers when the other one-half is conducting, thereby enhancing the power transfer characteristics and efficiency of said transmitter and eliminating current spiking and current drain in said transformer.

2. The transceiver defined in claim 1 which further includes a receiver section operatively associated with said transmitter section on a single semiconductor die and operative to receive and process bi-phase data RX IN and RX IN which is received from the transmitter section of a like transceiver, said receiver section comprising:

a. a differential input-differential output amplifier stage connected to receive said bi-phase data RX IN and RX IN,
b. a balanced differential filter stage connected to receive the differential output signal from said amplifier stage and having closely controlled thresholds and noise immunity characteristics which may be established using thin film resistors and MOS capacitors

Assignee: Medtronic, Inc.

Current U.S. Classification
307/475; 307/454; 307/296.6; 307/480; 455/63; 375/26

International Classification
H03K 19092

Search within this patent

Search

Citations

Patent Number	Title	Issue date
4614882	Bus transceiver including compensation circuit for variations in electrical characteristics of components	Sep 30, 1986
4955075	Battery saver circuit for a frequency synthesizer	Sep 4, 1990
4955080	Selectively called receiver	Sep 4, 1990
4967108	Differential-time-constant bandpass filter using the analog properties of digital circuits	Oct 30, 1990
4984291	Coded communication system with shared symbols	Jan 8, 1991
4989261	Power supply intercept with reference output	Jan 29, 1991
5014343	Squelch-tail eliminator	May 7, 1991

deposited on an external surface of said semiconductor die,
c. a differential comparator stage connected to receive the differential output signal from said balanced differential filter stage and operative to generate bi-phase output signals when the signals received at said balanced differential filter stage exceed a certain threshold and fall within a prescribed filter bandwidth, and
d. first and second output logic drivers connected, respectively, to first and second outputs of said differential comparator stage for generating RX DATA OUT and RX DATA OUT signals for use in controlling an associated computer.

3. The transceiver defined in claim 1 wherein said logic stage includes:

a. an EXCLUSIVE OR gate having first and second input terminals for receiving thereat TX IN and TX IN bi-phase input data and further having its output conductor connected as one input to a conventional OR gate, and
b. in INHIBIT data line connected as a second input terminal to said conventional OR gate, whereby TX IN and TX IN data are applied directly to said first and second wave shaping stages, and the output signals from said conventional OR gate are also connected as input signals to said first and second wave shaping stages within said low power transmission timer.

4. The transceiver defined in claim 3 wherein said low power transmission timer further includes a wave shape interface stage connected to receive input signals from said conventional OR gate and further having first and second output data lines connected, respectively, to said first and second wave shaping stages for controlling the timing of said first and second wave shaping stages and ensuring that one of said wave shaping stages has been completely turned off before the other wave shaping stage turns on.

5. The transceiver defined in claim 4 wherein each of said output current drivers includes a plurality of parallel connected driver transistors connected to each of two primary windings of a center tapped output transformer, with all of said parallel connected transistors being operatively driven by a current source output terminal in each of said wave shaping stages, respectively, whereby said current driver transistors are operative to dynamically drive the two primary center tapped transformer windings out of phase and further wherein each transistor in each of said current driver output stages is completely

Referenced by

Patent Number	Title	Issue date
5357151	Intrinsically safe logic and-circuit having two inputs	Oct 18, 1994
5812595	Waveform shaping circuit for a multiplexed information bus transmitter	Sep 22, 1998
5939753	Monolithic RF mixed signal IC with power amplification	Aug 17, 1999
6026286	RF amplifier, RF mixer and RF receiver	Feb 15, 2000
6728368	Apparatus and method for a highly efficient low power driver for a central office ADSL system	Apr 27, 2004

turned off before transistors in the other current driver output stage are turned on.

6. The transceiver defined in claim 5 wherein each current source output terminal of each of said wave shaping stages is driven by a lateral PNP transistor having bias and control circuitry connected thereto for overdriving said lateral PNP transistor to rapidly turn it on and thereafter providing rapid base discharge to said lateral PNP transistor to rapidly turn off said lateral PNP transistor to thereby enhance the switching speed thereof and further to prevent said lateral PNP transistor from turning back on when said current source output terminal of each of said wave shaping stages is driven below ground potential.

7. The transceiver defined in claim 6 wherein said logic input stage includes:

a. first and second data channels connected, respectively, to drive first and second output switching transistors, and
b. first and second DC bias and current source strings interconnecting said first and second output switching transistors between a supply voltage terminal and a point of reference potential, said first and second DC bias and current source strings further having first and second output current source nodes therein so that said first and second output switching transistors are operative to alternately source current out of each of said output current source nodes to one of said first and second wave shaping stages when said switching transistor is turned off and operative to source current into said first and second output switching transistors when said output switching transistors are turned on, thereby dynamically driving said first and second output current source nodes in said DC bias and current source strings dynamically out of phase.

8. The transceiver defined in claim 7 wherein said wave shape interface stage further includes threshold level control and sync pulse timing circuitry useful as an interface circuit for controlling the timing of signals in said first and second wave shaping stages and including, in combination:

a. an input voltage reference node referenced to the bandgap voltage of silicon,
b. a DC bias and current source string connected between a low voltage supply terminal and a point of reference potential and being connected to said input voltage

reference node, said DC bias and current source string further having a plurality of reference voltage junctions therein set at different pre-established DC bias voltage levels,
c. first and second pairs of output transistors each connected between one of said reference voltage junctions on said DC bias and current source string and first and second wave shape driving nodes for generating thereat a ramp voltage having voltage swings between different levels controlled by the voltages at said reference voltage junctions, and
d. an output reference voltage terminal connected to a different reference voltage junction in said DC bias and current source string and being operatively connectable to a threshold reference voltage device in each of said wave shaping stages, whereby the ramp voltage at each of said first and second wave shape driving nodes and applied, respectively, to each of said first and second wave shaping stages is operative to swing above and below said threshold reference voltage at said output reference voltage terminal and thereby in turn switch on and off an active data channel in each of said first and second wave shaping stages.

9. The transceiver defined in claim 8 which further includes a receiver section operatively associated with said transmitter section on a single semiconductor die and operative to receive and process bi-phase data which is received from the transmitter section of a like transceiver, said receiver section comprising:

a. a differential input-differential output amplifier stage connected to receive said bi-phase data,
b. a balanced differential filter stage connected to receive a differential output signal from said amplifier stage and having closely controlled thresholds and noise immunity characteristics which may be established using thin film resistors and MOS capacitors deposited on an external surface of said semiconductor die,
c. a differential comparator stage connected to receive a differential output signal from said balanced differential filter stage and operative to generate bi-phase output signals when the signals received at said balance differential filter stage exceed a certain threshold and fall within a prescribed filter bandwidth, and
d. first and second output logic drivers connected, respectively, to first and second outputs of said differential comparator stage for generating bi-phase output data signals for use in controlling an associated computer.

10. An all monolithic transceiver having a receiver section therein which includes:

a. a differential input-differential output amplifier stage connected to receive said bi-phase data RX IN and RX IN,
b. a balanced differential filter stage connected to receive the differential output signal from said amplifier stage and having closely controlled thresholds and noise immunity characteristics which may be established using thin film resistors and MOS capacitors deposited on an external surface of said semiconductor die,
c. a differential comparator stage connected to receive the differential output signal from said balanced differential filter stage and operative to generate bi-phase output signals when the signals received at said balanced differential filter stage exceed a certain threshold and fall within a prescribed filter bandwidth, and
d. first and second output logic drivers connected, respectively, to first and second outputs of said differential comparator stage for generating RX DATA OUT and RS DATA OUT signals for use in controlling an associated computer.

11. Logic circuitry for operation in a transmitter section of an all monolithic transceiver which includes, in combination:

a. first and second data channels connected, respectively, to drive first and second output switching transistors, and
b. first and second DC bias and current source strings interconnecting said first and second output switching transistors between a supply voltage terminal and a point of reference potential, said DC bias and current source strings further having first and second output current source nodes therein operative to alternatively source current out of each of said current source nodes to a wave shaping stage when a switching transistor connected thereto is turned off and further operative to source current into said switching transistor connected thereto when said switching transistor is turned on.

12. The logic circuitry defined in claim 11 which further includes means for biasing said first and second switching transistors at a voltage which is referenced to the bandgap voltage of silicon, thereby rendering said logic circuitry relatively insensitive to variations in temperature and voltage coefficients within said logic circuitry.

13. The logic circuitry defined in claim 11 which

further includes an INHIBIT channel connected in parallel with said first and second data channels, said INHIBIT channel being further connected to both of said first and second output switching transistors and operative to turn off said first and second output switching transistors in response to INHIBIT signals applied to said INHIBIT channel.

14. The logic circuitry defined in claim 13 which further includes means for biasing said first and second switching transistors at a voltage referenced to the bandgap voltage of silicon, thereby rendering said logic circuitry relatively insensitive to variations in temperature and voltage coefficients with said logic circuitry.

15. Wave shaping circuitry useful in the connection and operation with bi-phase data channels of a transmitter section of a monolithic transceiver and operative to ensure that one of said data channels has been completely turned off before the other channel of the transmitter turns on, said wave shaping circuitry including, in combination:

a. a data channel and a voltage reference channel connected to receive digital data and a threshold reference voltage, respectively, for activating said data and voltage reference channel when said digital input data and said voltage reference levels exist at certain values,
b. first and second lateral PNP output transistors connected to an output current source node for driving thereat a transceiver output stage when said first lateral PNP transistor is turned on and for turning off said output stage when said second lateral PNP output transistor is turned on and said first lateral PNP output transistor is turned off, and
c. control circuit means connected to said first lateral PNP output transistor for overdriving said first lateral PNP output transistor and rapidly turning it on and thereafter rapidly removing base charge from said first lateral PNP output transistor to rapidly turn it off and ensure that neither of said first and second lateral PNP output transistors is turned back on when said output current source node goes below ground potential.

16. The wave shaping circuitry defined in claim 15 wherein said control circuit means includes a third lateral PNP transistor connected to said first lateral PNP output transistor, and a turn off drive transistor connected in parallel with both said first and third lateral PNP transistors and operative to turn off and rapidly discharge said first and third lateral PNP transistors when said wave shaping

stage is being turned off.

17. The wave shaping circuitry defined in claim 15 which further includes:

a. differentially coupled transistor pairs connected to receive, respectively, reference voltage and digital input data applied to said wave shaping circuitry, and
b. first and second cascaded transistors connected between one transistor in said differentially coupled transistor pairs and a load resistor which in turn is connected to a supply voltage terminal, said load impedance operative to turn on said first and second cascaded transistors when said transistor pairs are switched and generate a voltage, delta V, across said load resistor which in turn is mirrored at a load resistor for said first lateral output PNP transistor and is operative to rapidly turn off said first lateral output PNP transistor when said wave shaping circuitry is being turned off.

18. The wave shaping circuitry defined in claim 17 wherein said control circuit means includes a third lateral PNP transistor connected to said first lateral PNP output transistor, and a turn off drive transistor connected in parallel with both said first and third lateral PNP transistors and operative to turn off and rapidly discharge said first and third lateral PNP transistors when said wave shaping stage is being turned off.

19. The wave shaping circuitry defined in claim 18 wherein said reference voltage terminal is connected through an input buffer transistor to a first plurality of emitter coupled NPN transistors and said digital input data is applied through a second buffer transistor to a second plurality of NPN emitter coupled transistors, with said first and second pluralities of NPN emitter coupled transistors being differentially switched into and out of conduction to thereby alternately drive said first and second cascaded transistors to conduction and non-conduction and thereby provide rapid overdrive and turn on of said first lateral output PNP transistor when said wave shaping circuitry is sourcing current out of said output current source node thereof and rapidly turn off and discharge said first lateral output PNP transistor when said wave shaping circuitry is being turned off.

20. An output current driver circuit for a monolithic integrated transceiver and operative to drive an inductive load such as one-half of the primary winding of a center tapped transformer, including, in combination:

a. a plurality of matched transistors connected in parallel and further connected between an input current source node and one end of a coil, and
b. bias circuitry connected to both the base and emitters of each of said plurality of matched transistors for controlling the DC operating bias on said plurality of matched transistors and setting the output current levels therefrom when each of said plurality of matched transistors is driven to conduction to provide output current to said coil.

21. The output current driver circuitry defined in claim 20 wherein each of said plurality of transistors is an NPN connected transistor, all having a common base input connection to a current source input node from a wave shaping stage.

22. The output current driver circuit defined in claim wherein said bias circuitry connected to said bases and emitters of each of said plurality of matched transistors includes:

a. a first plurality of emitter resistors connected between the emitters, respectively, of said plurality of matched transistors and an output coil, and
b. a plurality of base resistors connected, respectively, between each of the base connections for said plurality of matched transistors and the respective ends of each of said emitter resistors.

23. A threshold level control and sync pulse timing circuit useful as an interface stage for controlling timing in a connected wave shaping stage, including, in combination:

a. an input reference voltage node referenced to the bandgap voltage of silicon,
b. a DC bias and current source string connected between a low voltage supply terminal and a point of reference potential and also being connected to said input reference voltage node, said DC bias and current source string having a plurality of reference voltage junctions therein set at different pre-established DC bias voltage levels,
c. first and second output transistor pairs connected between one of said reference voltage junctions on said DC bias and current source string and first and second output wave shape driving nodes for generating thereat ramp voltages having control voltage swings which are in turn controlled by the voltage levels at said reference voltage junctions, and
d. an output reference voltage terminal

connected to another different reference voltage junction in said DC bias and current source string and being operatively connectable to a threshold reference voltage device in a following wave shape stage, whereby said ramp voltage at each of said first and second wave shape driving nodes and applied, respectively, to each of first and second wave shaping stages is operative to swing above and below the threshold reference voltage at said output reference voltage terminal and in turn switch on and off an active data channel in each of said wave shaping stages.

24. The threshold level control and sync pulse timing circuitry defined in claim 23 wherein said DC bias and current source string includes:

a. an input current source transistor connected to both a load impedance and to said input reference voltage node, and
b. a plurality of resistors and temperature compensating base emitter junctions connected in series between said input current source transistor and a point of reference potential and defining said plurality of reference voltage junctions within said current source of string which are useful for controlling the voltage levels at said first and second output transistor pairs and the voltage level at said output reference voltage terminal.

25. The threshold level control and sync pulse timing circuitry defined in claim 24 wherein:

a. said first and second wave shape driving nodes are connected, respectively, to output nodes of said first and second transistor pairs with each transistor in a transistor pair being alternately conductive to the exclusion of the other, and further with one transistor in each transistor pair being connected to a separate output wave shape control and timing voltage terminal which is also connected to drive a following wave shape stage, and
b. offset voltage means connected between said last named terminal and one of said voltage reference junction in said DC bias and current source string for providing a small offset differential in voltage bias between that applied to transistors in said first and second transistor pairs and that generated out at said output voltage reference terminal to ensure a solid switching action in said following wave shape stage.

26. A DC coupled differential input/differential output monolithic receiver including, in

combination:

a. a differential input/differential output first or input stage having differentially coupled input transistors connected to drive output buffer transistors,
b. a differential input/differential output second or intermediate filter stage having differentially coupled transistors connected to and driven by said output buffer transistors of said first stage and being further connected to differentially driven output buffer transistors, said second stage including a pair of balanced low pass filter networks connected between said buffer transistors in said input stage and said differentially coupled transistors in said filter stage and operative for establishing a predetermined gain versus frequency characteristic and roll-off out beyond a certain operating frequency, and
c. a differential input/differential output third or output window comparator stage connected to said output buffer transistors in said intermediate filter stage, said output window comparator stage including a differentially coupled transistor pair connected to a pair of current source transistors, and a pair of differentially driven output nodes connected between said pair of current source transistors and said differentially coupled transistors in said window comparator stage, said pair of current source transistors being further connected through a pair of load resistors, respectively, to a voltage supply terminal and establishing a desired output current level in signal swing at said pair of differentially driven output terminals of said window comparator stage.

27. The receiver defined in claim 26 which further includes current source transistors connected between all of said differentially coupled transistors in each of said stages and a point of reference potential and further being connected to a common bias node which is reference to the bandgap voltage of silicon.

28. The receiver defined in claim 27 wherein said pair of current source transistors in said window comparator stage are connected to a reference voltage node referenced to the bandgap voltage of silicon, and

b an additional pair of current source transistors connected to said differentially coupled transistors in said window comparator stage and optionally connected in parallel with existing current source transistors in said window comparator stage and further being

connected to either ground potential so as to operate as active current sources or being allowed to float or connected to a positive DC supply voltage for being effectively removed from said window comparator stage, whereby said optional pair of current source transistors in said window comparator stage are operative to change the resting DC levels and polarities at said differentially connected output terminals in said window comparator stage.

29. The receiver defined in claim 28 which further includes a pair of additional, balanced low pass filter networks connected at the outputs of said buffer transistors in said differentially connected filter stage and operative to provide an additional pole of roll-off at higher frequencies for said gain versus frequency characteristic of said receiver.

30. The receiver defined in claim 29 wherein each of said differentially coupled transistor pairs in each of said input, intermediate filter and output window comparator stages includes a common emitter resistor connected therebetween in order to set the proper threshold levels in each of these three stages and further operative to enable said stages to handle both large signal and small signal swings during the processing therethrough of antenna signals coupled to said first amplifier stage.

31. The receiver defined in claim 30 which further includes a pair of clamping diodes connected between said differentially coupled input transistors in said first amplifier stage and a point of reference potential and operative for clamping said differentially coupled transistors in said first stage when they are overdriven during the operation of an associated transmitter connected to the same coil as said receiver.

32. The receiver defined in claim 30 which further includes a pair of resistor networks connected between said differentially coupled input transistors in said first stage and a pair of input terminals operative for connection to an antenna, said pair resistor networks each having therein an insertable resistor which may be added or removed from said resistor networks to change the impedance thereof and accommodate variations in levels of signals received from said antenna.

33. A high speed and efficient transistor/transistor logic (TTL) output stage for a receiver section of a monolithic transceiver and operative to be driven by differential output signals from a window comparator stage, including, in combination:

a. input circuit means connectable to a pair of differential output nodes of said window comparator stage, and
b. non-saturating TTL output circuit means connected between said input circuit means and a TTL output terminal, said output circuit means having complementary switched output transistor pairs therein connected in tandem and operative for driving said output terminal between first and second logical output levels.

34. The TTL output stage defined in claim 33 wherein said complementary switched output transistor pairs are operative to drive said TTL output terminal between one base-emitter voltage drop, V.sub.BE, above ground and one V.sub.BE below a supply voltage for said output stage.

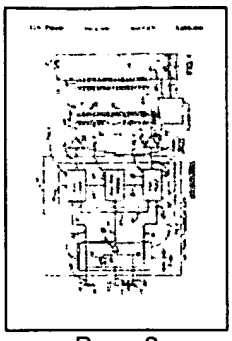
35. The TTL output stage defined in claim 33 wherein said output circuit means includes upper and lower complementary driven transistors within each of said transistor pairs and being alternately driven to conduction when the output logic swing at said output terminal is moving between two output logical levels.

36. The TTL output stage defined in claim 35 wherein said input circuit means is further connected to a reference voltage node which is referenced to the bandgap voltage of silicon and further includes in input NPN transistor connected to the output of said window comparator stage and an input PNP transistor connected to said reference voltage node.

37. The TTL output stage defined in claim 35 which further includes clamping circuit means connected between a strobe input terminal and said transistor pairs in said output circuit means and operative to disable said output circuit means upon receiving signals at a predetermined level from said strobe circuit means.

38. The TTL output stage defined in claim 37 wherein said input circuit means includes a first NPN input transistor connected to differential output nodes from said window comparator stage and a PNP input transistor connected to a reference voltage node referenced to the bandgap voltage of silicon, said input circuit means further including an enable/disable transistor being connected between said input PNP transistor and said clamping circuit means and further being operative to receive strobe signals to provide an additional degree of enabling and disabling capability for said TTL output stage by signals received from a strobe cell.

Drawings



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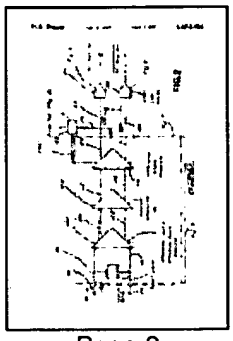

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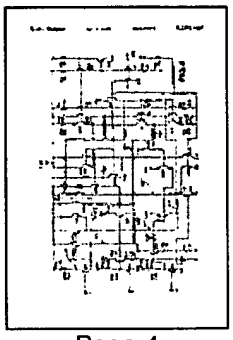

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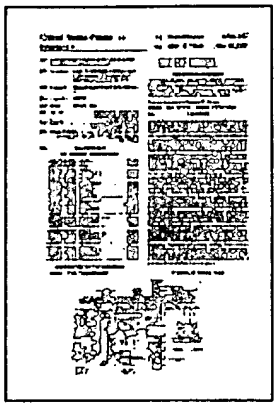
more »

Computer controlled multi-link communication system James E. Dahlquist et al

Patent summary



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Abstract | Drawing | Description | Claims

Abstract

A multi-link communication system includes a number of stations and interconnecting audio links under the control of a central computer. Each station is addressable by the computer for connecting selected stations to a selected audio link for establishing audio communication between stations. Each station has at least one corresponding access circuit for establishing an audio connection to a selected or preassigned link, and the connection is maintained by a corresponding memory circuit that is addressable by the computer. A group of output lines from the computer are used as select inputs to an analog multiplexer connecting a bidirectional control line to the selected access circuit for connecting or disconnecting the corresponding station and also for receiving connect or disconnect requests from the corresponding station. In a particular embodiment, the stations include multi-link dial and dialless telephones, single-link dialless telephones, and intercom speakers in an automati...

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Inventors: James E. Dahlquist, Peter C. Holtermann, Carl P. Rau
Assignee: Rauland-Borg Corporation

Current U.S. Classification
379/247; 379/263; 379/265; 379/269; 379/384

International Classification
H04M 322; H04Q 130; H04Q

Claims

What is claimed is:

1. A communication system comprising, in combination,

at least one audio link for establishing an audio communication path,
a plurality of stations for receiving and transmitting audio signals, and having means for requesting a connection to said audio link,
at least one respective access circuit being connected to each station, each access circuit including means for selectively connecting and disconnecting its respective station to the audio link, and also having means for receiving a request for connection from its respective station,
a computer for supervising the connecting and disconnecting of said stations to said audio link, and including means for addressing a selected one of said access circuits, interrogating the addressed access circuit to determine whether said addressed access circuit is receiving said request for connection, and in response to said interrogation commanding said addressed access circuit to selectively connect its respective station to said link, and means interconnecting said computer to said access circuits including a bidirectional control line for both conveying connection and disconnection commands from said computer to said access circuits and for conveying connection requests from said access circuits to said computer, and means for selectively connecting said control line to said addressed access circuit.

2. The communication system as claimed in claim 1 wherein said means for selectively connecting said control line includes at least one analog multiplexer having a multiplex terminal wired to said control line, and a plurality of select inputs wired to respective select lines from said computer.

3. The communication system as claimed

3545; H04Q 364

Search within this patent

Search

Citations

Patent Number	Title	Issue date
2258650	SIGNALING SYSTEM AND APPARATUS	Oct 14, 1941
2261243	TELEPHONE SYSTEM	Nov 4, 1941
2883472	MULTIPHONE FOR USE IN TELEPHONE SYSTEMS	Apr 21, 1959
2911477	MARKERS CONTROL FOR CROSSBAR AUTOMATIC TELEPHONE SYSTEM	(unknown)
2966554	AUTOMATIC TELEPHONE SYSTEM WITH PAGING EQUIPMENT	Dec 27, 1960
3342944	MULTICHANNEL INTERCOM SYSTEM WITH COMMON SIGNALING. CHANNEL	Sep 19, 1967
3350508	IMMEDIATE RINGING CIRCUIT FOR TELEPHONE SYSTEMS	Feb 19, 1952
3501596	CALL OFFERING CIRCUITS	(unknown)
3551601	EQUIPMENT FOR AUTOMATICALLY RETRYING CUSTOMER DIALED CALLS	(unknown)
3553385	QUEUING AND AUTOMATIC RETRY ARRANGEMENTS FOR COMMUNICATION	(unknown)

in claim 1, wherein said means for selectively connecting said control line include a plurality of analog multiplexers, each having a multiplex input wired in parallel to said control line, a plurality of select inputs wired in parallel to respective select lines from said computer, and an enable input receiving a respective enable signal from said computer.

4. The communication system as claimed in claim 3, wherein said means for selectively connecting said control line include at least one decoder having inputs connected to a plurality of respective select lines from said computer, and having at least one output connected to a respective one of said multiplexer enable inputs.

5. The communication system as claimed in claim 1, wherein said computer includes an input/output circuit wired to said control line and including means for selectively applying first and second voltage potentials to transmit connect and disconnect signals to said access circuits, and at least one voltage comparator responsive to the voltage on said control line for receiving said connection requests.

6. The communication system as claimed in claim 1, wherein said computer includes an input/output circuit wired to said control line, and said input/output circuit includes at least two voltage comparators for receiving both low and high priority connection requests.

7. The communication system as claimed in claim 1, wherein said stations include telephone stations and intercom stations.

8. A communication system for providing two-way communication between a telephone having a means for entering numbers, and a selected one of a plurality of intercom speakers being selected by entering a corresponding number from said telephone, said communication system comprising, in combination,

a voice controlled amplifier connecting said telephone to a speaker audio bus for establishing an audio communication path,
for each of said speakers, an access circuit including means for selectively connecting and disconnecting the

	SYSTEMS	
3584151	KENNETH L. KIFLAR	(unknown)
3660610	CONFERENCE CALL CIRCUIT	(unknown)
3678208	TERMINATING DUNCTORS TJ-I TJ-Z TJ-J TJ-X TJ-S TJ-G TJ-T TJ-B TJ-Z TJ-IOL	(unknown)
3697700	LINE HUNTING CIRCUITRY FOR COMMON CONTROL COMMUNICATIONS SWITCHING SYSTEM	(unknown)
3701853	SHEET L OF	Oct 3, 1972
3809824	(unknown)	May 1974
4064377	Electronic hybrid and hybrid repeater	Dec 20, 1977
4081614	Supervised single link telephone system	Mar 28, 1978
4180860	Display station having universal module for interface with different single loop controllers	Dec 25, 1979
4289934	Integrated automatic call distribution facility and PBX system	Sep 15, 1981
4351986	Electronic telephones with cooperative interaction between a master set and members' sets in a group	Sep 28, 1982
4559417	Method of setting operating data in a key telephone system	Dec 17, 1985
4570035	Programmable key telephone system	Feb 11, 1986
4605825	Function key assignments in a key telephone system	Aug 12, 1986

Referenced by

speaker to the speaker audio bus, a computer for supervising the connection and disconnection of said speakers to said speaker audio bus, and including means for receiving a number from said means for entering numbers, and addressing a corresponding one of said access circuits to connect its respective speaker to said speaker audio bus, and
means interconnecting said computer to said access circuits including at least one control line for transmitting connection and disconnection commands from said computer to said access circuits, wherein said connection and disconnection commands are in the form of pulses of a first and a second polarity, and wherein each access circuit has a latching relay being energized for connecting its respective speaker to said speaker audio bus by said pulse of said first polarity, and being energized for disconnecting its respective speaker from said speaker audio bus by said pulse of said second polarity, and
further comprising means for selectively connecting said control line to said addressed access circuit comprising an analog multiplexer, so that one control line carries the connection and disconnection commands to a number of access circuits.

9. The communication system as claimed in claim 8, wherein said control line is a bidirectional line for also transmitting connection requests from switches associated with said speakers to said computer, and wherein said computer repetitively interrogates said switches for displaying connection requests to the user of said telephone and interrogates a selected one of said switches by addressing said analog multiplexer for selectively connecting the selected switch to said control line.

10. The communication system as claimed in claim 9, wherein each speaker has associated with it two switches, a first one of which applies a first signal level to said control line when it is selected by said multiplexer and activated by a person to transmit a low priority connection request, and a second one of which applies a second signal level to said control line when it is selected by said multiplexer and activated by a person to transmit a high priority connection request, and wherein

Patent Number	Title	Issue date
4941171	Electronic private branch exchange	Jul 10, 1990
4991199	Computer and telephone apparatus with user friendly computer interface and enhanced integrity features	Feb 5, 1991
5008927	Computer and telephone apparatus with user friendly computer interface integrity features	Apr 16, 1991
5109219	Method and apparatus for controlling and adjusting the viewing angle of a liquid crystal display	Apr 28, 1992
5461668	Telephonic console with programmable nonvolatile personality memory and method	Oct 24, 1995
5485370	Home services delivery system with intelligent terminal emulator	Jan 16, 1996
5572572	Computer and telephone apparatus with user friendly interface and enhanced integrity features	Nov 5, 1996
5644730	Dual mode binary sensor for bus operation	Jul 1, 1997
5796832	Wireless transaction and information system	Aug 18, 1998
5870724	Targeting advertising in a home retail banking delivery service	Feb 9, 1999
5875242	Telecommunications installation and management system and method	Feb 23, 1999
6202054	Method and system for remote delivery of retail banking	Mar 13, 2001

said computer uses means for sensing and discriminating between the first and second signal levels in order to display both low and high priority connection requests to the user of said telephone.

11. A communication system comprising, in combination,

a plurality of audio links for establishing simultaneous and independent audio communication paths,
a plurality of telephones for receiving and transmitting audio signals, and including means for entering numbers for requesting connection to other of said telephones,
each of said telephones having an access circuit including means for selectively connecting and disconnecting the telephone to a selected one of the audio links, and
a computer for receiving the numbers entered by said means for entering numbers and in response thereto supervising the connection and disconnection of said telephones to said audio links,
wherein each access circuit includes a transformer for converting a balanced audio signal from the line of the telephone to an unbalanced signal having a ground which is common for the unbalanced signals from all of the telephones, the unbalanced signal being connected to a selected one of said audio links through an analog multiplexer integrated circuit having select inputs receiving link select signals from a latch circuit storing the link select signals and having received the link select signals from the computer.

12. The communication system as claimed in claim 11, wherein each of said access circuits further comprises a circuit including a memory element for receiving and storing connection and disconnection commands from said computer, and also including a circuit for detecting whether the corresponding telephone is on-hook or off-hook, and wherein said communication system further comprises a bidirectional multiplexed control line for sending connection and disconnection commands from said computer to selected ones of said access circuits, and for sending on-hook and off-hook signals from selected ones of the access circuits to said computer, and

	services	
6442532	Wireless transaction and information system	Aug 27, 2002
6681001	Computer integrated telecommunications systems and methods	Jan 20, 2004
6760419	Method and apparatus for interfacing a drive-thru intercom system with a telephone system	Jul 6, 2004
6832356	Gate driver for power device	Dec 14, 2004

wherein said communication system further comprises an analog multiplexer for accessing said selected ones of said access circuits and receiving said bidirectional multiplexed control line on a common multiplex terminal.

13. In an administrative communication system the combination comprising at least one dialable administrative telephone having dialing means, a plurality of dialless staff stations, and a control computer for supervising connections between the administrative telephone and staff stations, the administrative telephone being dialed to establish communication between a selected staff station and the administrative telephone, and the staff stations having switches for requesting communication with the administrative telephone, the control computer having means for scanning said switches to determine stations requesting communication, and at least one remote display being connected to said central computer and being provided for displaying numbers corresponding to the stations requesting communication, wherein binary data including said numbers are transmitted as a pulse-width modulated binary signal from said control computer to said remote display so that said remote display can be located at least one thousand feet from said control computer.

14. The combination as claimed in claim 13, wherein said display is mounted on said administrative telephone, and wherein said pulse-width binary signal is a balanced signal transmitted over a pair of wires in a phone line connecting said administrative telephone to said control computer, and wherein said display including circuits for demodulating and decoding said pulse-width modulated signal is powered by rectification and filtering of said pulse-width modulated signal.

15. The combination as claimed in claim 13, wherein the individual pulses in said pulse-width modulated signal are generated by execution of a sequence of successive steps in an interrupt program of said computer, and wherein only one of said pulses is generated each time that said interrupt program is executed.

16. In an administrative telephone and intercom system having a plurality of stations including multi-link dialable

telephones having dialing means, dialess multi-link telephones, dialess single-link telephones, and intercom speakers, connections between said stations being supervised by a control computer, each of said stations being selectively addressable by said control computer transmitting corresponding preassigned physical numbers to said respective stations, and a selected one of said stations being connected to a multi-link dialable telephone in response to dialing from said multi-link dialable telephone a preprogrammed architectural number corresponding to the physical number of the selected station, said control computer having data stored in electrically alterable memory for said physical numbers identifying the architectural number associated with each physical number and whether a multi-link dialable dialless telephone or single line telephone or intercom speaker is addressable at said physical number, at least one of said multi-link dialable telephones having an associated display for displaying numbers transmitted from said control computer, said control computer being programmed to receive numbers dialed from said telephone associated with said display to permit user programming of said control computer, a method of operating said control computer for user programming comprising the steps of:

(a) receiving a first number dialed from said multi-link dialable telephone associated with said display, testing the first number to determine whether the first number corresponds to a preassigned number for user programming, and upon receipt of said number for user programming thereafter
(b) receiving a second number dialed from said multi-link dialable telephone associated with said display to identify a physical number for which reprogramming of said electrically alterable memory is desired, and thereafter
(c) displaying said data stored in said electrically alterable memory associated with the physical number identified by said second number received in step b), and thereafter
(d) receiving a third number dialed from said multi-link dialable telephone associated with said display and changing said data stored in said electrically alterable memory in response

to said third number.

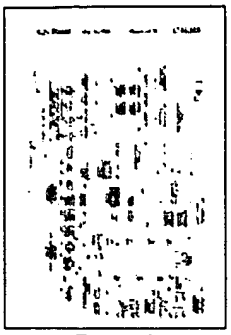
17. The method of operating said computer as claimed in claim 16, wherein the data for each physical number identifying whether one of said multi-link dialable or dialess telephone or single link telephone or intercom speaker is associated with the physical number is encoded as an ordered series of bits, and wherein said step (c) of displaying said data displays said data encoded as an ordered sequence of digits or blanks, a digit or blank being selectively displayed in response to whether a corresponding bit is set or cleared, and wherein said step (d) of receiving said third number comprises receiving a digit dialed from said telephone and changing the value of the bit corresponding to the digit dialed from said telephone.

18. The method of operating said computer as claimed in claim 16, wherein said data stored in said electrically alterable memory further includes data identifying whether both one of said intercom speakers and one of said telephones is associated with a physical number, and wherein said computer directs calls to said physical number to said speaker associated with said physical number, unless said telephone associated with said physical number goes off-hook during a call directed to said physical number whereupon the call is directed to said telephone associated with said physical number.

19. The method of operating said computer as claimed in claim 16, wherein a physical number is associated with both one of said speakers and one of said telephones, and said data stored in said electrically alterable memory and associated with said physical number includes a bit identifying whether a call directed to the physical number is first directed to the speaker or is first directed to the telephone associated with the physical number.

20. The method of operating said computer as claimed in claim 16 wherein mechanically operated electrical switches are provided for preselecting the physical numbers associated with particular ones of the telephones and speakers.

Drawings



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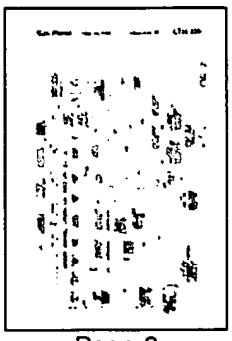

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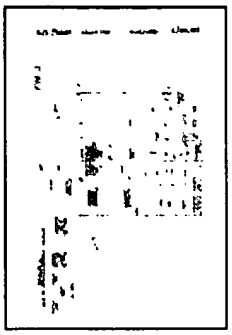

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